Indian Journal of Science and Technology, *Vol 8(14), 61848, July 2015*
ISSN (Print) : 0974-6846
ISSN (Online) : 0974-5645

Low Power Estimation on Test Compression Technique for SoC based Design

P. Raja Gopal[1*] and S. Saravanan[2]

[1]VLSI Design, SASTRA University, Thanjavur, 613401, India; rajagopal.075ece@gmail.com
[2]School of Computing, SASTRA University, Thanjavur, 613401, India; saran@core.sastra.edu

Abstract

Test power dissipation is one of the major challenging task in System on Chip (SoC). The objective of the paper is to reduce the power consumption during testing in VLSI testing field. This paper analyzes the test power consumption for the test data to get the low power consumption by using switching activity. The Low Power Transition – X filling (LPT-X) method is proposed to reduce the transition switching where unknown bits were filled. Weighted Transition Metric (WTM) method used to estimate low test power. This paper approach achieves reduction of average power consumption by LPT-X filling method. Using ISCAS89 benchmark circuits the experimental results were conducted and achieves 83 percent of reduced average test power.

Keywords: Low Power Transition (LPT), Switching Activity, System on Chip (SoC), Test Power, Weighted Transition Metric (WTM), X-Filling

1. Introduction

The Intellectual Property (IP) core embedded in System on Chip (SoC) circuit becomes more complex with large volume of test sets. Several factors like test data volume, test power and area determine the complexity. The volume of the test data is of major concern in testing over SoC, several IP blocks are the major constituents of a typical SoC. Each of these blocks must be trained with larger test patterns that are precomputed. Test power is another factor which causes dynamic power dissipation for test patterns, which is reduced due to switching activity between the test data patterns. Linear decompression, broadcast scan based and code based schemes are some schemes reduces the volume of test data.

Linear decompressed shifts data linearly using LFSR reseeding and XOR operations[1] to encode the test data. Broadcast scan based schemes are used to shift the data from single scan chains to multiple scan chains. It reduces the decompression area of the test data. In Code based schemes the test data is partitioned and encoded with special symbols. The symbols are then replaced with code word to obtain the compressed data. Larger the test data more memory of Automatic Test Equipment (ATE) is required, resulting in reduced compression ratio. The compressed data not only reduces ATE memory but also gives low test power. While testing the chip on SoC power consumption is necessary since excessive power can cause high power consumption which damages the Circuit Under Test (CUT) to be tested. More Power is consumed in test mode than in normal mode. The switching activity causes the power consumption in test patterns[2]. This test power is reduced by minimizing the switching activity. The unknown bit locations are filled with zeros and ones, Weighted Transition Metric is used to decrease the test power[3].

Recently, several techniques are used to reduce the test data pattern volume, resulting in reduction memory requirements of ATE. Data compression technique has test independent methods which run with 1's and 0's. The run length used for better compression is 0's. FDR code[4] is a variable to variable run length code with the runs

*Author for correspondence

of 0's. It has prefix and tail with same size of bit to form code words which are assigned with frequency of variable length. The results are varies with intensive change of inputs. The EFDR code (extended FDR code) is also similar to FDR but runs with both 1's and 0's[5]. To determine run length of 1's extra bit 0 is replaced with 1 at starting of code word formation and the test power is high.

Low-power scan operation[6] achieved by compression test vectors. The compressed data will be saved in the memory of ATE. Again the data is recovered by the on-chip decoder. Mostly it doesn't need the structural information of the embedded cores. Low shift power[7] shows the compression and decompression which is based on structure of test data. It gives the relation between signaling the probability of test data, partition of the scan flip flops had a skewed signaling used to higher the compression ratio. This reduced by inserting the scan flip flops adjacently for the scan chains gives 50 percent of low shift in power with low area overhead.

A unique approach to minimize the test data volume and power[8] is obtained by TRP to decrease power and volume of the test pattern. It is based run length code to increase compression ratio and mapping the unknown bits to zeros and ones in reducing the scan average power. In paper [9] partitioning based WTM was discussed. Low power switching activity is found by identifying the partitioning blocks with transition and nontransition test patterns. Shift in power was focused by paper [10] with threshold method of unspecified test patterns. Appropriating indexing and encoding is in this method to reduce switching activity of the test patterns. RL_HF encoding[11] is a mixed of run length and huffmann based coding the bits are filled with zeros and ones to make dynamic switching activity to reduce power consumption of scan cells. This method is used to find the test compression and scan power.

Low power selective compression[12] forms the data into patterns of different stages then applying the code word method to get compression ratio. The data is taken linear of splitting the test data patterns process to take more time. Then binary values are used to map the test sets, to determine testing power. Coloring algorithm method is used in paper [13] which promises for low power test pattern compaction. Scan power minimization [14] can be used to modify the scan data chain by inserting logic gates in scan path, leading to reduced transition during shifting of cycles and reducing test power. Forms of matrix bounds are introduced to test the stimulus and responses of scan chains. This method used to minimize the overall testing power of scan paths. XOR network based scan power reduction was identified in paper [15] where travelling salesman problem is used to find out the least number of test pattern switching.

The block merging eight coding technique in [16] shows row-column reduction routine to reduce test data volume. This technique splitting the total data into block sizes and encodes the data to achieve higher compression ratio. Test set compaction is generated by Mintest[17] by full scanned ISCAS89 bench mark circuits. The paper [18] shows the various power consumption methods to achieve low power under testing. A new scheme of test data compression based on Equal-Run-Length Coding (ERLC)[19] to reduce the test data volume by running the length of zeros and ones in equal patterns and applied for the low power for the circuits under testing to achieve low average power. The paper [20] uses GDI T-flip flop method is reduce the power in CMOS circuits in Vlsi field and achieves low area.

2. Power Estimation

The compressed test data on power consumption during testing is determined. This paper shows how the test power is consumed by filling unknown bits with appropriate binary values for the merged data for [16]. In SoC consumed power is addressed into two types named as dynamic power and static power. When transitions are occur from one to zero and zero to one the dynamic power is taken into account. While the process of power consuming leakage power caused by static power which is not considered in this paper. Test patterns can be compressed as per the code word mentioned in Table 1 is as shown in paper [16]. The test power consumption occurs due to transitions of test patterns that has more switching activity. Power estimation methods based switching activity of circuits.

On using the Weighted Transition Metric (WTM)[18] test power consumption is estimated. The WTM models for the power consumption not only depends on the transitions occurred for test patterns, it also depends on various positions. Weighted transition metric is mainly associated to switching activity during scan chain operation for circuit under test. WTM for the scan vector is applied by considering scan length of the circuit. Let us consider a scan test vector $V_p = V_{p,1}, V_{p,2}, V_{p,3}, \ldots V_{p,l}$ and length of the test vector is l. WTM for test patterns is calculated as,

Table 1. Test Pattern with its codeword as in paper[12]

Test Patterns	Type	Codeword
01X1X 10X1X	Inverse Compatible	0 010
10XX1 10X11	Half Compatible	0 11+ bit/2
1X0X0 0X100	Half Inverse	0 10+bit/2
00000 1X101	0U	0 01100+bit/2
11111 10X1X	1U	0 001101+bit/2
1X01X 00000	U0	0 01110+bit/2
X0X10 11111	U1	0 01111+bit/2
X101X 0X101	UU	0 00+bit

$$WTM_p = \sum_{q=1}^{l-1} \left(V_{p,q} \oplus V_{p,q+1}\right) * (l-q) \quad (1)$$

If total set of test data contains N vectors V_1, V_2, V_3, ... V_N then the total power is obtained by summing the all the vectors 1 to N. The average power is obtained by dividing the total power by total number of test sets. The peak power is obtained as the highest power in all the test vectors. The total power, average power and peak power is given as,

$$Power_{total} = \sum_{p=1}^{N_v} \sum_{q=1}^{l-1} \left(V_{p,q} \oplus V_{p,q+1}\right) * (l-q) \quad (2)$$

$$Power_{average} = \frac{\sum_{i=1}^{N_v} \sum_{j=1}^{l-1} \left(V_{p,q} \oplus V_{p,q+1}\right) * (l-q)}{N} \quad (3)$$

$$Power_{peak} = \left(1 \le p \le l^{max} WTM_p \rightarrow \right. \quad (4)$$

3. Low Power Transition - X Filling

Filling up of unknown bits with appropriate binary bits 0's and 1's for the test patterns to measure the power of the test data. Considering the test patterns having '0', '1' and 'X' where 'X' is unknown bit to be filled. It is filled randomly with the adjacent values by 0's and 1's. Suppose the X is the starting value, fill the bit with next bit value. The test power is consumed with weighted transitions of scan chain.

The sequence of data is divided into blocks and filling the data. Considering an example of the test data 001X0X101X110XXX11XX is divided into two blocks of bit size as 10 and is formed as 001X0X101X and 110XXX11XX. The divided blocks containing X is filled as 0011001011 and 1100001111 and applying the Weighted Transition Metric to calculate power. This is caused by switching activity between bits transferred. The data having the length 10, the power is 23 for first value and 12 for the next value; this is achieved from equation (1). Some of the example data is given to fill the X value.

Table 2 shows the filling of X data with suitable binary values and applying weighted transition metric. The power is calculated and the values are given as, overall power is 79, avg power is 15.8 and highest (peak) power is 23 from equations (2), (3), and (4).

4. Experimental Results

The test power for [16] compression method and for five large ISCAS89 bench mark circuits is analyzed in this section. The weighted transition metric is used for estimating total power, average power by using above equations. The unknown bits are padded with suitable binary bits. The average power is the main consumption power for the test power. Some statistics are given for the bench mark circuits

Table 3 represents test patterns, total number of bits contained in a circuit and the percentage of unknown care bits for five large scan ISCAS89 bench mark circuits.

Table 2. LPT-X Filling bit with WTM

Test patterns	LPT-X Filling	WTM
T1=1X0X1X0X00	1100110000	18
T2=110XXXX0X1	1100000001	9
T3=X01X0X101X	0011001011	23
T4=X101XX00X1	1101110011	21
T5=00X001X101	0000011101	8

Table 3. ISCAS89 Benchmark circuits with Don't Care Bit

Circuits	Test Patterns	Test Bits	Total Data	Don't Care Bit (%)
s9234	159	247	39273	73.01
s13207	236	700	165200	93.15
s15850	126	611	76986	83.33
s38417	99	1664	164736	68.08
s38584	136	1464	199104	82.28

Table 4 represents the comparison between the total power and average power for uncompressed and compressed data for the five circuits of [16]. The average power is reduced to 191 units after compressing the test data leads to get low average power. The total power is also reduced for test data.

Table 5 represents the comparison results of average power of [16] with existing methods like Mintest[17], OC_SP[3], FDR[4], EFDR[5] and ERLC[19]. The eight coding technique gives better average power on comparing to existing methods. Such that the average power is reduced while testing the circuit.

Table 4. Comparison of Total and Average Power

Circuits	Total Data (T_D)	Uncompressed[16]		Compressed[16]	
		Total Power	Average Power	Total Power	Average Power
9234	39273	629314	3957	621380	3908
13207	165200	1825366	7734	1584864	6715
15850	76986	1702737	13513	1732992	13753
38417	164736	11636595	117541	11711814	118301
38584	199104	11649193	85655	11528990	84731
Average	--	5488641	45680	5436008	45489

Table 5. Comparison of Average Power with Existing Methods

CIRCUITS	MINTEST[17]	OC_SP[3]	FDR[4]	EFDR[5]	ERLC[19]	LPT-X Filling
s9234	14630	8132	5692	3469	3500	3908
s13207	122031	17809	12416	8016	8115	6715
s15850	90899	24850	20742	13394	13450	13753
s38417	601840	578450	172665	117834	120775	118301
s38584	535875	108050	136634	89138	89356	84731
Average	273055	147458	69630	46370	47039	45489

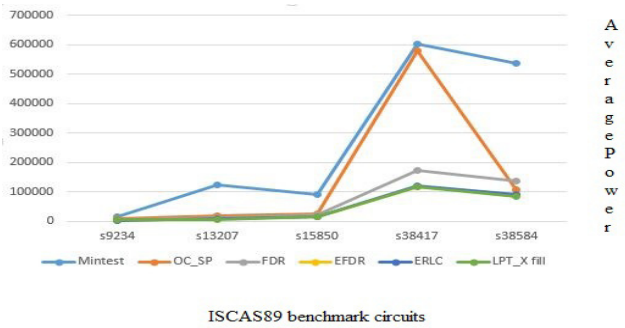

Figure 1. The graph shows comparison of Average power with other existing methods.

5. Conclusion

This proposed method shows reduction of test power in scan based design. LPT-X filling method is used for filling unknown bits to produce reduced switching. This paper approach achieves reduction of average power consumption by using LTP-X filling method for paper [12] method. Proposed LTP-X filling method with merged test patterns is applied to Weighted Transition Metric and gives low switching power. Average power is reduced up to 83 percent when compared with other existing methods.

6. References

1. Touba NA. Survey of test vector compression techniques. IEEE Transaction Computer-Aided Design Integrated Circuits Systems. 2006; 23:294–303.
2. Mu SP, Chao MC-T. Theoretical analysis for low-power test decompression using test-slice duplication. 28th VLSI Test Symposium. 2010; 13:147–52.
3. Bhavsar KA, Mehta US. Analysis of don't care bit filling techniques for optimization of compression and scan power. International Journal of Computer Applications. 2011; 18:887–975.
4. Chandra A, Chakrabarty K. Frequency Directed Run-length (FDR) codes with application to system-on-chip test data compression. Proceedings of 19th IEEE VLSI Test Symposium. 2003; 52:42–7.
5. EL-Maleh AH. Test data compression for System-On-Chip using extended frequency directed run-length code. IET computers & Digital Techniques. 2008; 2:155–63.
6. Czysz D, Kassab M, Lin X, Mrugalski G, Rajski J, Tyszer J. Low-power scan operation in test compression environment. IEEE Transaction Computer-Aided Design Integrated Circuits Systems. 2009; 28:1742–55.
7. Wang SJ, Li KSM, Chen SC, Shiu HY, Chu YL. Scan-Chain partition for High Test-Data Compressibility and Low Shift Power under Routing Constraint. IEEE Transaction of Computer- Aided Design Integrated Circuits Systems. 2009; 28:716–27.
8. Chandra A, et al. A unified approach to reduce SOC test data volume, scan power and testing time. IEEE Transaction Computer-Aided Design Integrated Circuits Systems. 2003; 22:352–62.

9. Saravanan S, Upadhyay HN. Transition Based input test vector partitioning for low power switching activity. Journal of Theoretical and Applied Information Technology. 2011; 32:146–51.
10. Saravanan S, Elakkiya G. Test data compression based on threshold method for power reduction research. Journal of Applied Sciences, Engineering and Technology. 2012; 4:2100–4.
11. Nourani M, Tehranipour M. RL-Huffmann encoding for test compression and power reduction in scan application. ACM transaction Des AUTOM Electron Systems. 2005; 10:91–115.
12. Sivanantham S, Malick PS, Raja Paul Perinbam J. Low Power Selective Compression for scan based test application. Computers and Electrical Engineering. 2014; 40:1053–63.
13. Saravanan S, Upadhyay HN. Achieving low power test pattern by efficient compaction method for SoC design. Journal of Artificial Intelligence. 2012; 5:244–8.
14. Sinanoglu O, Orailoglu A. Scan Power minimization through Stimulus and Response transformations. Design Automation and Test in Europe Conference and Exhibition Proceedings. 2004; 1:404–9.
15. Saravanan S, Sowmiya G, Sai RV. Design and analysis of reduced test power in scan based design. International Journal of Engineering and Technology. 2013; 5:692–5.
16. Wu TB, Liu HZ, Liu PX. Efficient test compression technique for SoC based on block merging and eight coding. Journal Electron Test. 2013; 29:849–59.
17. Hamzaoglu SI, Patel SJH. Test set compaction algorithms for combinational circuits. IEEE Transactions Computer-Aided Design Integrated Circuits System. 2000; 13:957–63.
18. Basker P, Arulmurugan A. Survey of low power testing of VLSI circuits. IEEE International Conference on Computer Communication and Informatics. 2012; 10:978.
19. Zhan W, El-Maleh A. A new scheme of test data compression based on equal-run-length coding (ERLC). The VLSI Journal of Integration. 2012; 45:9–18.
20. Umarani P. A high performance asynchronous counter using area and power efficient GDI T-Flip Flop. Indian Journal of Science and Technology. 2015; 8:382–6.