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Optimization of SRAM Array Structure for Energy Efficiency Improvement in Advanced CMOS Technology

J. S. Ashwin* and J. S. Praveen

AMET University, Chennai, India; jsashwin2010@gmail.com, Praveenjs1985@gmail.com

Praveenjs1985@gmail.com

Abstract

This paper explores the design and analyze of SRAM array structure to decrease the power dissipation and to increase the energy efficiency. The SRAM array structure with high energy efficiency can be achieved with wider array structure with fewer rows than columns particularly in low supply voltage. The proposed analysis shows that the SRAM array structure optimization can improve the energy efficiency up to 20% at the same supply voltage.

Keywords: Optimization, SRAM Array, Energy Efficiency, CMOS Technology

1. Introduction

In ultra low power application, high energy efficiency is a paramount design constrains. In such application, Static Random Access Memory (SRAM) plays a key role in energy consumption due to high cell density for computational power improvement. Portable electronic devices have very low power requirement to maximize the battery lifetime. Various device-circuit-architectural level techniques have been implemented to minimize the power consumption[1].

The traditional approach to obtained minimum energy consumption is by reducing the supply voltage below the device threshold voltage[2-4]. However this technique generates degradation in following parameter, i.e., cell stability, noise margin and a strong sensitivity to process-voltage-temperature[3]. So this approach is not much effective in the minimization of SRAM energy and it also increases the delay exponentially.

Evan and Franzon[5] investigate the SRAM array structure to decrease the energy consumption, and the minimum energy consumption was found to be non-square array structure. Normally the array structure was designed with equal number of rows and columns. The taller array structure which had more rows than column was introduced to minimize the energy consumption by dominating the dynamic power consumption. While this taller array structure increases the memory access time and reduces the speed of operation and it is applicable only for high performance application.

The total energy analysis for SRAMs over active and ideal operating modes and array biasing for energy minimization are developed [11].

Designing of six transistors SRAM cell operating in low voltage application faces various challenges, one of which is the cell stability during read operation. So the separate read and write port[6] of different SRAM cells (7T, 8T and 9T) can overcome the stability related limitations of 6T SRAM cells, which makes the SRAM cell a promising candidate for such low voltage levels [7-10]. A dual port sram cell is used in the sub-array for our simulations, since it has been widely employed for the ultra low voltage operation.

**Author for correspondence*

The proposed design was explained in section II. The analysis of different SRAM cell structures (6T, 7T, 8T, and 9T) was discussed in section III. The total energy consumption of SRAM sub-array was derived analytically in section IV. Section V analysis the SRAM array structure for energy minimization and its simulation results were discussed in section VI. Finally, section VII summarizes and concludes this work.

2. Proposed Design

The proposed design, analyzes the 16 bit SRAM array structure for minimum energy consumption by using different SRAM cells (6T, 7T, 8T, 9T). Here the number of rows and that of columns can be changed while their product remains constant. The array can be optimized by reducing the number of rows than columns, this wider array structure which have minimum SRAM cells in a column and its flow of leakage current through the bit-line has been reduced when compared to the normal array structure, and this approach mainly focused on ultra low-power application. Low power CMOS transistor using 0.12µm technology was used in this design. Digital schematic and micro wind v3.1 tools were used for this simulation.

A SRAM sub-array with the density of 16 bit was used in this paper, in normal array structure for the density of 16 bit array have four rows and four columns (4x4), by altering the number of rows and columns without changing the cell density the energy efficiency can be improved.

3. Analysis of Different SRAM Cell

Before analyze the array structure, different SRAM cell structure should be analyzed to choose the best one.

A. 6T SRAM CELL

Conventional 6T SRAM cell shown in Figure 1 were used normally in array structure which have less layout area. A 6T SRAM cell consists of two cross coupled cmos inverters, the content in the bit cell can be accessed by two NMOS access transistor. Using single word line read and write operation can be done.

However, the potential stability problem with this design arises during read and write operation, where the cell is most vulnerable towards noise and thus the stability of the cell is affected. If the cell structure is not designed properly, it may change its state during read and write operation. Due to various drawbacks of the 6T SRAM cell, separate read and write port SRAM cell were used in this paper.

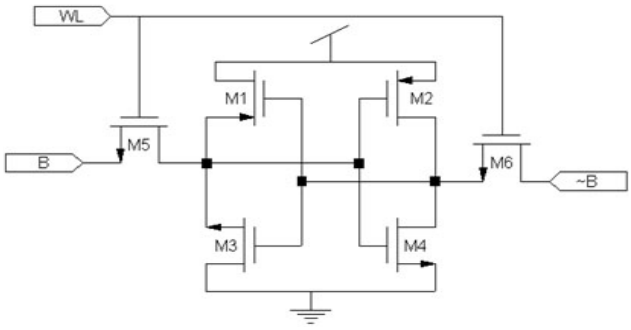

Figure. 1 Conventional 6T SRAM cell

B. 7T SRAM CELL

The single ended 7T SRAM cell in Figure 2 consists of single-ended write port and a separate read port. An extra transistor is added in the pull-down path of one of the inverters. During read mode the extra transistor is turned off, and data are isolating the corresponding storage node from Vss.

Write mechanism is same as in a 6T SRAM cell. It provides a read-disturb-free operation and increase the read stability. The limitation was that the area overhead from the conventional 6T SRAM cell.

C. 8T SRAM CELL

A dual-port 8T cell is created by adding two transistors to conventional 6T SRAM cell is shown in Figure 3. The read operation is entirely decoupled from the write operation. Transistor M7 and M8 are employed to reduce the leakage current during read operation. A memory cell having a dual-port which increases write ability and read stability.

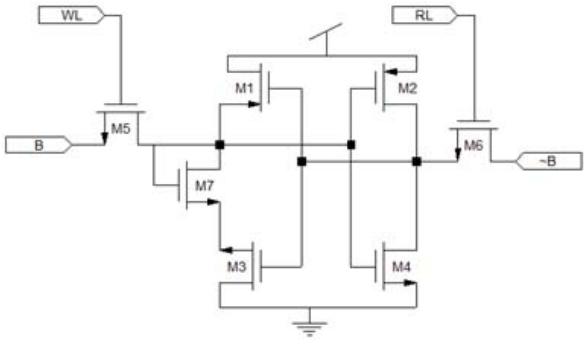

Figure. 2 Single ended 7T SRAM cell

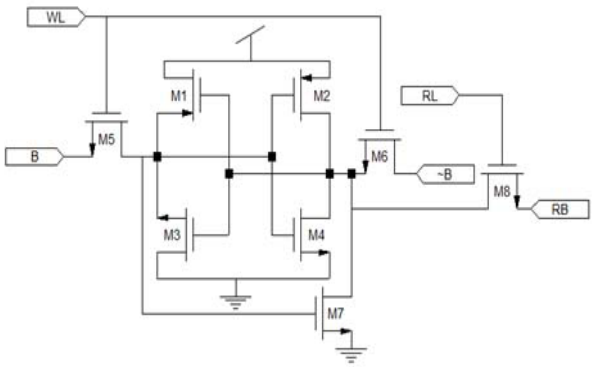

Figure. 3 8 T SRAM cell

It has some drawbacks when the column for read (RL) is not accessed, the leakage current through m7 may cause a severe voltage drop at the read bit-line, leading to large power dissipation especially in the deep submicron nano range.

D. 9T SRAM CELL

In 9T SRAM cell separate read port is used to decouple the read and write operation which is similar to the 8T SRAM cell is shown in Figure 4. Stacked read access transistors are used to reduce the leakage current. The word line for read has been also is distinct from the write word line. This circuit enhanced data stability. The 9T SRAM cell completely isolates the data from the bit lines during a read operation.

The idle 9T SRAM cells are placed into a super cutoff sleep mode, thereby reducing the leakage power consumption as compared to the standard 6T SRAM cells. This circuit shows reduced leakage power and enhanced data stability and provides less power dissipation.

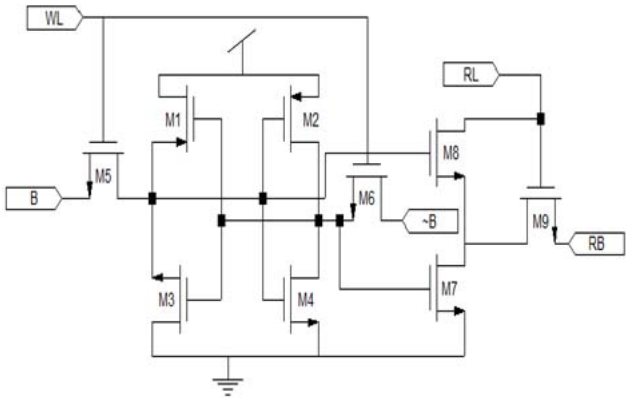

Figure. 4 9 T SRAM cell

By analyzing the simulation results of different SRAM cell structures (6T, 7T, 8T and 9T) using micro wind v3.1, the 9T SRAM cell consumes less power due to its separate read port architecture. It overcomes the stability-related limitations of other SRAM cell, which makes the 9T SRAM cell a promising candidate for such low voltage levels. A 9T SRAM cell is used in the sub-array of our simulations since it has been widely employed for ultra low-voltage operation.

4. SRAM Energy Model

In this section, the total energy consumption of 9T SRAM sub-array structure is modeled. When the supply voltage is low enough making the static energy component dominating, the total SRAM energy (E_{total}) is given by

$$E_{total} = j \times k \times I_{lcell} \times t \times V_{DD} + (j \times .5C_{RBL} \times V_{DD}^2 + K \times C_{WBL} \times V_{DD}) + (j + C_{RBL} \times V_{DD}^2 + K \times C_{WBL} \times V_{DD}) \quad (1)$$

Here j is the number of rows, k is the number of columns, I_{l_cell} is the leakage current in an SRAM cell, t is the cycle time of the SRAM cell, C_{WBL} is the write bit-line capacitance per cell, C_{RBL} is the read bit-line capacitance per cell, and V_{DD} is the supply voltage.

In the energy equation, it is assumed that the probabilities of data "1" and those of the data "0" are equal and are 0.5. The dynamic energy component is mainly determined by the bit-line capacitance, while the static energy component coming from the leakage current is determined by the memory density. The effect of the read and write operations on the leakage current of the accessed row and column are insignificant. SRAM energy is a function of multiple variables such as supply voltage, capacitance, performance, temperature, workload, and organization. SRAM energy minimization has to be conducted while considering the entire afore mentioned component carefully. I_{l_cell} can be obtained by following expression:

$$I_{l_{cell}} = \frac{W \mu_n C_{ox} (V_{gs} - V_t)^2}{L^2} \quad (2)$$

Where, μ_n = 0.06 m^2/v-s is the mobility of electron, $C_{ox} = \varepsilon_0 \varepsilon_r$ is the gate capacitance per unit area, W is the width of access transistor of the SRAM cell, L is the length of the access transistor of the SRAM cell. V_{GS} = 0.9v is the gate

to source voltage of the access transistor in the SRAM cell and V_t= 0.4v is the threshold voltage of the transistor.

Write bit-line capacitance (C_{WBL}) and Read bit-line capacitance (C_{RBL}) can be obtained by:

$$C_{WBL} = \frac{WLe_0 e_r}{T_{ox}} \; C_{WBL} = \frac{5WLe_0 e_r}{T_{ox}} \qquad (3)$$

Where, W is the width of the MOS device, L is the length of the MOS device Tox = 2E-9 is the oxide thickness, ε_0 = 8.85 E-12 F/m is the absolute permittivity, ε_r = 3.9 (no unit) in case of SiO2 is relative permittivity.

An analytical expression for the energy consumption of 9T SRAM sub-array structure has been derived. The expressions are useful in predicting the effect of the parameter as well as in optimizing the design of the SRAM array structure. Based on a layout all parasitic capacitances of the bit-line, are included in the analytical expression. In our simulation all transistors in the SRAM structure have fixed size for different memory array size and the results obtained using micro wind v3.1. To simulate the SRAM array structure we use 1.2v supply voltage and the threshold voltage for NMOS transistor and PMOS transistor is 0.4v and -0.4v respectively.

5. Analysis of SRAM Array Structures for Energy Minimization

The 16 bit SRAM sub-array structure for minimum energy consumption using different SRAM cell structure (6T, 7T, 8T and 9T) were analyzed in this section.

Energy consumption is related to static and dynamic power dissipation. However, in the SRAM array for ultra low-power applications, the changes in the array structure are limited and following challenges were needed to meet in the designing process to minimize this energy. Minimum static energy can be achieved with an SRAM array structure with less number of rows than columns. But the minimum dynamic energy can be achieved with an SRAM array structure with more number of rows than column.

Due to these limitations, the number of rows and column were needed to select carefully. An SRAM sub-array with the density of 16 bit was used, in normal array structure for the density of 16 bit array have four rows and four columns (4x4), by altering the number of rows and columns without changing the cell the energy efficiency can be improved.

In this design 9T SRAM cell was used to architect the 2x8 array structure, to design this array structure the peripheral circuit like row decoder, pre-charge circuit, sense amplifier and Read/Write driver were used to implement the memory architecture.

In the proposed optimized array structure, only two rows are present which reduced the leakage current. Because in the read operation a single column is activated, in that column only two cells has been activated and the leakage current of that two SRAM cell can flow through that bit-line.

For 4x4 array structure the flow of leakage current through the column line of the four cells is larger, that lead to large power dissipation, but on proposed design the leakage current flow is minimized and that optimized the power dissipation.

The energy components (i.e., static energy and dynamic energy) of the SRAM array structure for determining the significance of each component on the energy minimization were analyzed. At a given supply level, changing SRAM array structure can also alter the SRAM energy.

6. Simulation Results

All the circuits were simulated using 0.12µm CMOS technology on micro wind v3.1. Figure 5 is depicting the power consumption of the different SRAM cell. 9T SRAM cell shows the least power consumption over other SRAM cell.

Figure 6 shows the power consumption of different 16 bit SRAM sub-array. 9T SRAM array structure shows the least power consumption over other SRAM array structure.

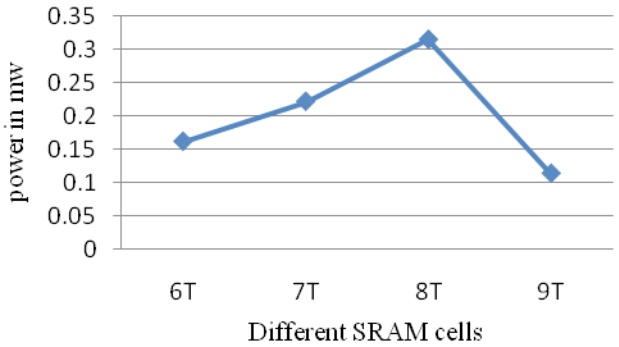

Figure. 5 Power consumption comparison of different SRAM cell structure

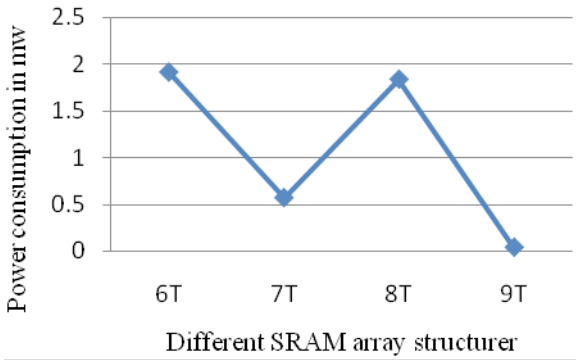

Figure. 6 Power consumption of different SRAM array structure

Figure 7 Demonstrates the energy consumption of existing and proposed 16 bit 9T SRAM array structure. Energy was minimized by optimizing the SRAM array structure.

Simulation results reveal that wider array structures provide higher energy efficiency at low supply voltage. However, the energy variation of the structure is not at all smallest. Smaller energy variation can be obtained by lowering the number of cells per bit beyond the optimal value, which will result in higher mean energy. The simulation results shown here match the analytically derived results in section IV.

7. Conclusion

This paper analyzed the 16 bit SRAM sub-array structure for minimum energy consumption by using different SRAM cell structure (6T, 7T, 8T and 9T) using micro wind v3.1 at 0.12µm CMOS technology. While normal 4x4 array structure using 9T SRAM cell consumes 30.5µw at 1.2V biasing voltage, the proposed 2x8 wider array structure shows better improvement which consumes 24.6µw at 1.2V biasing voltage. This change is mainly driven by the increased portion of SRAM in nano scale CMOS technology at low voltage. The simulation result explores that the power consumption of proposed wider array structure is minimized up to 20%, when compared to the traditional array structure using 9T SRAM cell at the same supply voltage.

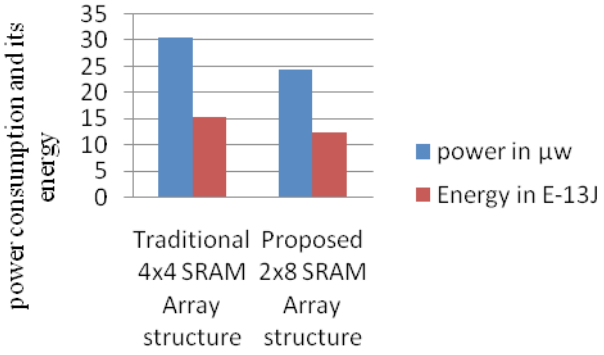

Figure. 7 power and energy consumption of existing and proposed system

8. References

1. K. Roy and Prasad, Low power CMOS VLSI Circuit Design, 1sted. New York: Wiley, 2000.
2. S. Cserveny, L. Sumanen. J. M. Masgonty and C. Piguet, "Locally Switched and limited source-body bias and other leakage reduction techniques for a low power embedded SRAM," IEEE Trans. Circuits Syst. II, Exp. Briefs, 2005;52,(10), 636–640.
3. B. H. Calhoum and A. Chandrakasan, "A 256kb subthreshold SRAM using 65nm CMOS," in Proc. Int. Solid-State Circuit Conf., 2006, 2592–2601.
4. B. H. Calhoum and A. P. Chandrakasan, "A 256-kb 65-nm sub-threshold SRAM design for ultra-low-voltage operation," IEEE J. Solid-State Circuits, 2007; 42(3), 680–688,
5. R. J. Evans and P. D. Franzon, "Energy consumption modeling and optimization for SRAM's," IEEE J. Solid-State Circuits, 1995;30(5), 571–579.
6. L. Chang, R. K. Montove, Y. Nakamura, K. A. Batson, R. J. Eickemever, R. H. Dennard, W. Haensch, and D. Jamsek, "An 8T-SRAM for variability tolerance and low –voltage operation in high-performance cache," IEEE J. Solid-State Circuits, 2008; 43(4), 956–963.
7. V. Joshi, R. Kanji, and V. Ramadurai, "A novel column-decoupled 8T cell for low-power differential and domono-based SRAM design," IEEE Trans. Very Large Scale Integr. (VLSI)Syst., 2011;19(5), 869–882.
8. B. Zhai, L. Nazhandali. J. Olson, A. Reeves, M. Minuth, R. Helfand, S. Pant, D. Blaauw, and T. Austin, "A 2.60pJ/Instsubthreshold sensor processor for optimal energy efficiency," in VLSI Symp. Tech. Dig., 2006;154–155.
9. A. Wang and A. Chandrakasan, "A 180-mV sub threshold FFT processor using a minimum energy design methodology," IEEE J. Solid-State Circuits, 2005; 40(1), 310–319.
10. A. T. Do, J. Y. L. Low, Z. H. Kong, X. Tan, and K.S.Yeo, "An 8T differential SRAM with improved noise margin for bit-interleaving in 65nm CMOS," IEEE Trans. Circuits Syst. I, Reg. Papers, 2011; 58(6), 1252–1263.
11. M. Naveen Varma "analysis towards minimization of total SRAM energy over active and ideal operating modes," IEEE Trans. Very Large Scale Integ,. (VLSI) Syst., 2011; 13(9) 1695–1703.