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A 1.5V CMOS Transconductor using adaptive biasing and its application

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Abstract

A low-voltage CMOS transconductor is designed in 0.35µm standard CMOS technology. The proposed circuit uses adaptive biasing linearization method to achieve better linearity in low voltage applications. Simulation results using HSPICE show a total harmonic distortion of -71 dB at 1.25 MHz for a 400 mV peak to peak input voltage. The total power consumption is only 45 µW with 1.5 V power supply. The circuit can be used in the implementation of membership functions or fuzzifiers in analogue and mixed-signal neuro-fuzzy systems.

Keywords: Adaptive biasing, High linear, Low-voltage, Low-power, Transconductance, Fuzzifier.

Introduction

Linear CMOS transconductors are versatile analog building block that find wide, but not exclusive, use in the implementation of continuous-time filters, data converters, fuzzy controllers or V-I converters for interfacing with current mode signal processing circuit (Sánchez-Sinencio *et al*, 1989; Valburg & van de Plassche, 1992; Sasaki *et al*, 1992; Thomsen & Brooke, 1993). Often in these applications the input transconductor determines the overall linearity of the system. Modern fabrication technologies and wireless applications also require low supply voltage and low power consumption, which make it difficult to achieve transconductors with high linearity and low supply voltage over a reasonable input range.

Consequently, several linearization techniques have been proposed in literature to enhance the linearity of MOS transconductors (Krummenacher & Joehl, 1988; Kuo & Leuciuc, 2001; Worapishet & Nephaphan, 2003; Kachare *et al.*, 2005a). The reported linearization techniques include: cross-coupling of multiple differential pairs, adaptive biasing, source degeneration (using resistor or MOS transistor), shift level biasing, series connection of multiple differential pairs and pseudo-differential stages (using transistor in the triode region or in saturation). Although all these techniques enhance the linearity, they are not well suited for low-voltage operation.

In this paper, a novel low-voltage high-linear CMOS transconductance block is proposed. The proposed circuit uses supply voltages 1.5V which is lower than most previous proposals. The circuit uses the adaptive biasing technique to improve the linearity.

In low-voltage applications, furthermore, it can be employed for all mentioned applications where a highly accurate voltage to current conversion should be realized.

Low voltage linear transconductor design

In this section, we will firstly review adaptive biasing linearization technique which is previously reported (Nedungadi & Viswanathan, 1984). In this technique an adaptive biasing current source is used to cancel the nonlinearity of the simple MOS differential pair. The principals of this technique are discussed and the mathematical equations of this technique are presented. Then the novel linear MOS transconductor is presented.

Fig.1.The simple differential MOS transconductor

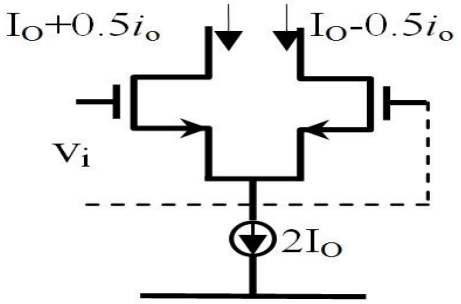
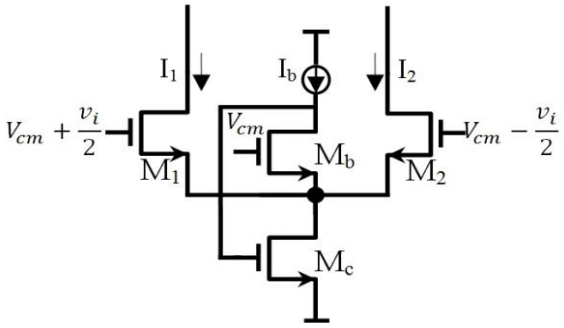


Fig. 2. Adaptive bias current generator



Adaptively biased MOS Transconductors

Considering quadratic *i* - v characteristics for the MOS transistors and neglecting the channel length modulation effect, the simple differential MOS transconductor (Fig.1) has a transfer characteristic given by

$$i_o = \frac{1}{2}kV_1\sqrt{\frac{\varepsilon I_0}{k}} - V_1 \qquad (1)$$

Where k represents the transconductance parameter ($k = \mu C_{ox}$)

Better linearity can be achieved for large effective

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gate-to-source voltages $V_{GSeff} = V_{GS} - V_{TH}$. For low-voltage applications this constitutes a major drawback Furthermore, large transconductance values can be obtained only by using large bias currents and large area transistors; however this changes cause to enlarge the power consumption and active area.

One of the topologies for linearization of the transfer characteristic of MOS transconductors is using the adaptive biasing current source.

The idea is using a dynamic bias current containing an input dependent quadratic component to cancel the nonlinear term in equation (1). Hence, if the bias is defined as equation (2),

(l_o = l_o + (2)

And put this equation in equation (1) the transfer characteristic becomes linear and could be realized according to equation (3)

$i_o = \sqrt{2k} l_o$ (3)

*The novel low-voltage circuit for generating the adaptive bias current***:** Fig. 2 shows the new low-voltage circuit for generating the adaptive bias current.

Assuming the same sizes for M_1, M_2, it can be easily shown that:

$$i_1 = \frac{1}{2}k_1\left(V_{cm} + \frac{v_i}{2}V_{cm} + V_{Gsb} - V_{th}\right)$$
$$= \frac{1}{2}k_1\left(\frac{v_i}{2} + V_{Gsb} - V_{thb}\right) \quad (4)$$

Where k_1 is the transconductance parameter of input devices, M_1 and M_2, ($k_1 = k_2 = \mu C_{ox}$)

Similar attempt for I_2 terminates to equation (5):

$$i_2 = \frac{1}{2}k_2\left(\frac{-v_i}{2}V_{cm} + V_{Gsb} - V_{th}\right) \quad (5)$$

Replacing V_{GSb} as a function of the bias current I_b

$$V_{Gsb} = V_{th} + \sqrt{\frac{2l}{\mu Cox}} \quad (6)$$

The following expression result:

$$i_2 = \frac{1}{2}k_2\left(\frac{v_i}{2} + \sqrt{\frac{2I_b}{\mu c_{ox}\frac{W_b}{L_b}}}\right) \quad (7)$$

$$i_2 = \frac{1}{2}k_2\left(\frac{-v_i}{2} + \sqrt{\frac{2I_b}{\mu c_{ox}\frac{W_b}{L_b}}}\right) \quad (8)$$

The current passing through M_C is equal to the sum of I_1, I_2 and I_b as clarified in the equation (9):

$$I_c = I_1 + I_2 + I_b = +I_b + \frac{1}{2}k_1\left(\frac{v_i^2}{2} + \frac{4I_b}{\mu c_{ox}\frac{W}{L}}\right) \quad (9)$$

As seen in (9), the current of M_C is expressed in quadratic relation with the input differential voltage.

If a copy of the current of M_C is mirrored into the tail current of basic differential pair which is discussed former in section 2.1, equation (10) can be concluded from combination of equations (1) and (9):

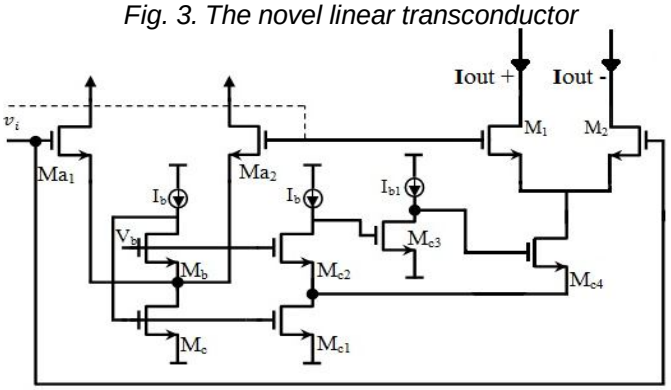
$$i_o = \frac{1}{2}kv_i\sqrt{\frac{g}{k}I_b + \frac{16k_1}{k_b}I_b + \frac{2k_1}{k}v_i^2} - \quad (10)$$

Where $k = \mu C_{ox}$ is the transconductance of basic differential pair, $k_1 = \mu C_{ox}$ is the transconductance of the adaptive biasing differential pair and $k_b = \mu C_{ox}1$ is the transconductance of the transistor. If $k_1 = 0$ the transfer characteristic becomes completely linear according to relation (11):

$$i_o = \frac{1}{2}kv_i\sqrt{\frac{g}{k}I_b + \frac{g}{k_b}} \quad (11)$$

The novel linear MOS transconductor

Fig. 3. The novel linear transconductor



We proposed a new MOS transconductor that uses the linearization approach presented above. The proposed circuit consists of 3 main blocks; an adaptive biasing current generator, a high performance current mirror and a main differential pair (Fig.3). M_{C1}- M_{C4} Form a high performance current mirror. (Ramirez-Angulo *et al.*, 2005) This circuit copies the dynamic current that produced by the adaptive bias current generator circuit which is formed by Ma_1, Ma_2, Mb and Mc into the source of the transistors of main differential pair with source degeneration transistor which is formed by M_1- M_2.

M_b , current source I_b and V_b forces the V_{DS} voltage of the transistor M_C to a constant value. A replica of this circuit is used to force the V_{DS} voltage of the transistor M_{C1} to be equal to that of the transistor M_C.

To have high output impedance, the output cascade transistor M_{C4} is driven by the drain of transistor M_{C2}. As the polarity in the drain of transistor M_{C2} is reversed, an inverting stage is required to drive the gates of transistor M_{C4} .This Inverting stage provides additional gain-boosting, which increases the output impedance. The inverter amplifier has been implemented by means of transistor M_{C3} and biasing current I_{b1}.

The minimum supply voltage is limited by the path formed by I_b, M_b and M_C , so the minimum supply voltage is

$V_{DD}^{min} = V_{GSC} + 3V_{DSbat}$ (12)

where V_{GSC} is gate-source voltage of M_C , V_{DSbsat} is the minimum voltage drop in current source and can be as

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Fig. 4. Post layout simulated DC transfer characteristic

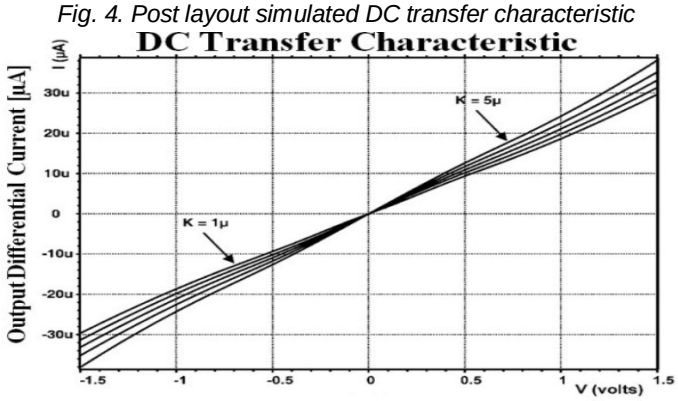


Fig. 5. Simulated output spectrum for 1.25 MHz and 400mV peak to peak input

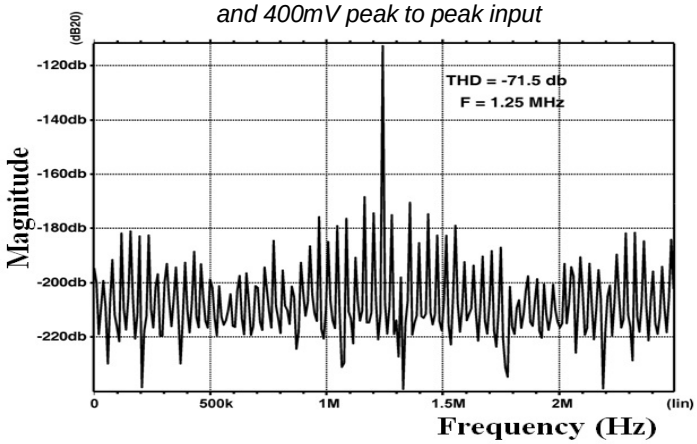


Fig. 6. Simulated THD for different frequencies: ▪ 125 KH_Z; × 1.25 MH_Z

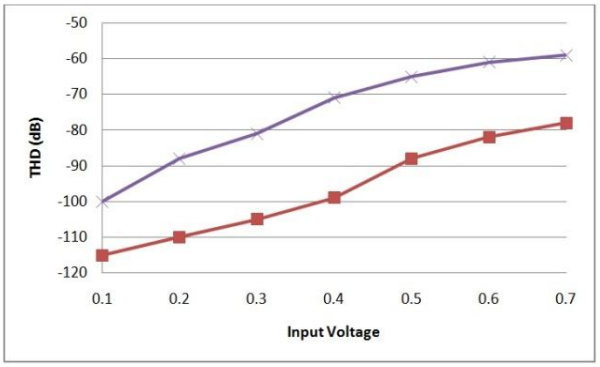


Fig. 7. Fuzzification of an input variable using membership function

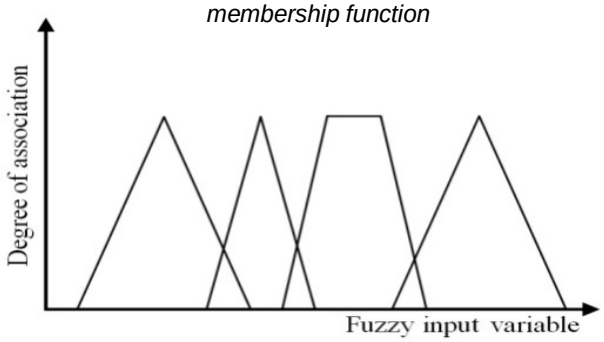


Fig. 8. (a) block diagram of fuzzifier (b) output characteristic of fuzzifier

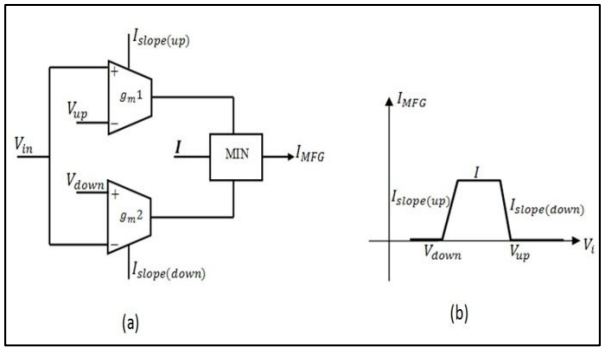


Fig. 9. The proposed low-voltage MIN circuit

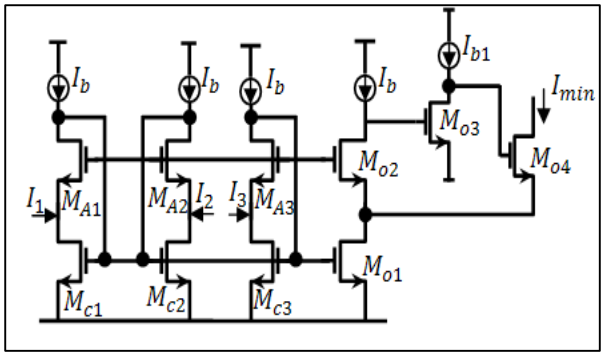


Fig. 10. Slope tunability of low-voltage fuzzifier

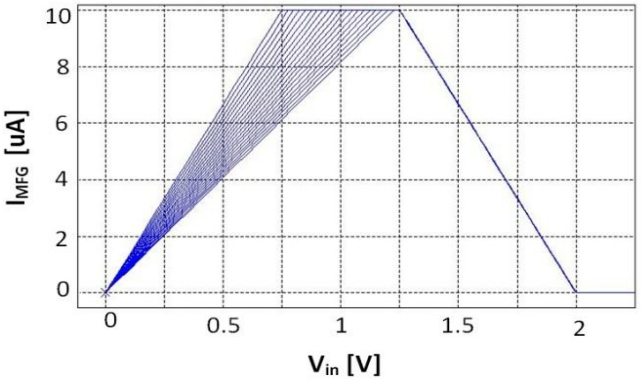
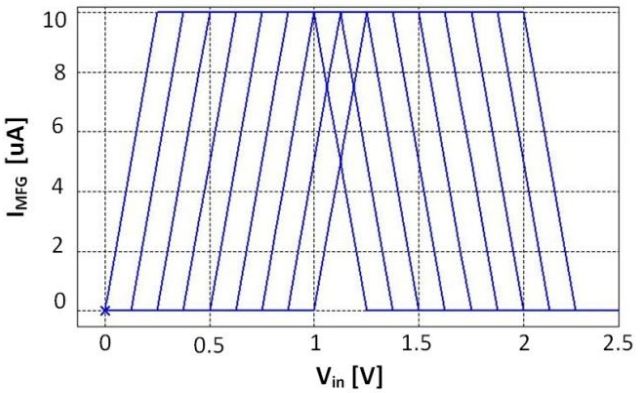


Fig. 11 Width tunability of low-voltage fuzzifier



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small as 0.15V in 0.35µm CMOS technology, V_{th} = 0. V for NMOS ,so

$V_{DD}^{min} = V_{th} + 3V_{DSsat} = 0.65 + 3 \times 0.15 = 1$

We have selected V_{DD}=1.5 V in order to have an appreciable voltage swing.

Simulation Result

The proposed transconductor was laid out in standard 0.35µm CMOS technology. Post layout simulations from extracted circuit were performed for a 1.5 V supply using HSPICE and level 49 parameters (BSIM3V3). Fig.4 shows DC characteristic of proposed transconductance circuit. This simulation results is obtained for 5 bias currents from 1 µA to 5 µA which is Specified in the Fig.4.

Note that high linearity was obtained, which was also confirmed by the total harmonic distortion. A -71 dB was obtained for a 400 mV peak to peak differential input voltage at 1.25 MHz. Fig. 5 shows the frequency spectrum of the output signal for a 1.25 MHz sinusoidal input signal with 400 mV peak to peak voltage. Fig. 6 shows the total harmonic distortion (THD) for different frequencies. The total power consumption of the circuit (using bias current of I_b = 3 µA) is only 45 µw.

Application

In this section, an application of the designed transconductor is presented.

Fuzzifier

The fundamental operation in fuzzy logic is fuzzification which consists of the determination of the degree of association of a variable to a fuzzy set (Zadeh, 1965) and is implemented by means of fuzzifier. This circuit provides a nonlinear relation that measures the compatibility of an object with the concept represented by a fuzzy set. Usually, fuzzifiers have a triangular or trapezoidal shape and, in order to guarantee general application, it needs to have programmable parameters (horizontal position, height, width and edge slope) (Kachare *et al.*, 2005b) (Fig.7).

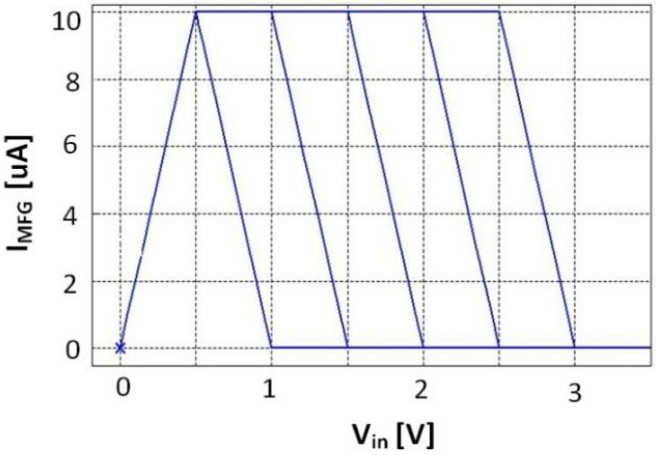
The proposed transconductor can find application in the implementation of fuzzifiers in fuzzy systems**.** Using two instances of transconductor in the Fig.3 and a minimum current selector circuit, a trapezoidal or triangular transconductor characteristic can be generated (Fig.8).

This block consists of two transconductors. One creates a positive ramp and the other creates a negative ramp, one defines the V_{up} and the other defines V_{down} , also each transconductor can independently define the slope of the up and down part via bias current I_b , then outputs go through a minimum current selector circuit which takes the minimum of them to construct a trapezoid output current. The new low voltage MIN circuit is designed for implementing a low-voltage fuzzifier (Fig.9).

The proposed circuit has 3 input branches and each branch consists of a current sensing transistor M_{Ci} and a voltage follower M_{Ai} while the gates of transistors M_{Ai} are connected to a common-mode constant voltage V_b .V_{GS} voltages of all M_{Ci} transistors are equal and proportional to minimum of input currents of I_1, I_2, I_3. This condition drives them to have different V_{DS} voltage. Since they (M_{C1}, M_{C2} and M_{C3}) have different V_{DS} voltage, the voltage follower of all branches (M_{A1}, M_{A2} and M_{A3}) are turned off with the exception of voltage follower in the loosing branch that has the minimum of input currents I_1, I_2 and I_3.

This transistor remains ON and with M_{O1}- M_{O4} forms a high performance current mirror that can copy the minimum current to the output.This MIN circuit also defines the fuzzy one level for whole MFG circuit. By choosing the value of **I** for the fuzzy one value we also can cut the output signal at the desired level, in other words for selecting **I** value, we can use the most linear part of the output signal.The proposed fuzzifier was laid out in standard 0.35µm CMOS technology. Fig.10, 11 and 12 show SPICE simulation of the low-voltage fuzzifier. All the parameters are independently tunable.

Fig. 12. Position tunability of low-voltage fuzzifier



The proposed low-voltage fuzzifier has the following advantages.

- It allows full and independent programmability of all parameters (horizontal position, height, width and edge slope).
- The circuit is able to operate at lower supply voltage than most pervious works. This aspect decreases the power dissipation of the proposed circuit. Moreover, the speed of proposed circuit is increased due to the fact that the parasitic capacitances have to be charged to less value in compare to previously reported circuits.

Conclusion

A novel low-voltage CMOS circuit for the Implementation of tunable transconductance with high linearity has been introduced. The circuit operates at a low supply voltage (1.5 V) with only 45 µW of quiescent power consumption. The proposed circuit uses adaptive biasing linearization method to enhance the linearity Simulation result shows -71 dB of THD for 400 mV amplitude of input signal at 1.25 MHz which confirmed the functionality of the proposed circuit. The circuit can be used for the implementation of fuzzifier in fuzzy systems.

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The proposed fuzzifier circuit has independently adjustable height, slope, position, and width of the trapezoidal function and has been verified by simulation results.

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