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Fuzzy Logic Controller Based IDVR in IEEE 30 Bus System for Voltage Sag Compensation

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Abstract

Objectives: Fuzzy logic controller based IDVR in IEEE 30 bus system for voltage sag compensation is proposed in this paper. **Methods/Analysis**: Closed loop control technique (PI, PID, FOPID and FUZZY) is implemented to analysis the dynamic perform of the system. Measurable parameters such as steady state error, peak time, and rise time, settling time and voltage profile of above controllers are simulated and compared using MATLAB/SIMULINK. **Findings:** The comparison results reveal that, a time domain specification is improved and steady state error is decreased. **Novelty/Improvements:** FUZZY logic based IDVR system has been implemented to improve the dynamic performance of the system.

Keywords: Fuzzy, FOPID, IEEE30, IDVR, PI, PID, Voltage Sag

1. Introduction

The power quality problem is becoming a major concern in the power system networks. Present days a power system networks are subjected to many power quality problems because of the increases in nonlinear loads. Among them the voltage sag is that the main downside inferred within the power quality networks, concerning eighty percentages of power issues within the grid network is because of the voltage sag. This paper provides resolution to the on top of downside by style of custom power devices that is IDVR. Among all the facts devices IDVR provides economical compensation reactive power because of voltage sag. Simulation and performance analysis of power quality improvement in distributed network using various custom power devices[1]. The IDVR is derived from the IPFC, where IPFC is the uni-directional device for the injection of reactive power by a DC voltage stored in a battery converted to AC by using a VSI .It is done between any one of the feeder. Whereas in IDVR the bidirectional flow and control of reactive power is achieved if any one of the feeder is an outage the compensation is done by IDVR using the bidirectional flow. Voltage Sag mitigation in two bus multi-line Distribution System using closed loop Controlled IDVR[2]. Neuro fuzzy controlled multi-level inverter based DVR and DSTATCOM for voltage sag mitigation[3]. Contingency studies for nine bus distributed system using IVDFC[4]. The above discussed literature review exhibits that the fuzzy logic controller is not enforced in IEEE30 bus system with IDVR for voltage sag mitigation. The system of the paper is as follows: Section II deals with system description. Section III provides the design of various closed loop controller. Section IV shows simulation results and discussion.

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2. System Configuration

The system configuration of the existing and proposed method are presented here. Figure 1& 2 exhibits the graphical diagram of distributed IEEE thirty bus system. The existing model has 6 generator buses and 20 load buses. If voltage dip occurs in any one of the load bus, entire distributed system will be affected.

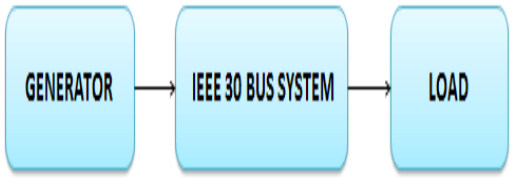

Figure 1. Block Diagram of Distributed Thirty Bus System.

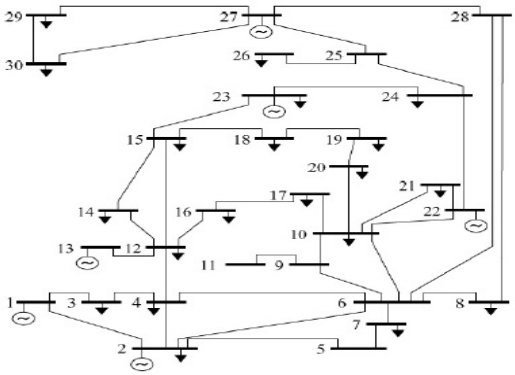

Figure 2. Graphical Diagram of IEEE 30 Bus System.

The pictorial diagram of novel method is shown in Figure 3. Proposed closed loop system with IDVR is employed to inject the reactive power in distributed line to increase the dynamic response of the system. Figure 4 shows the circuit diagram of IDVR.

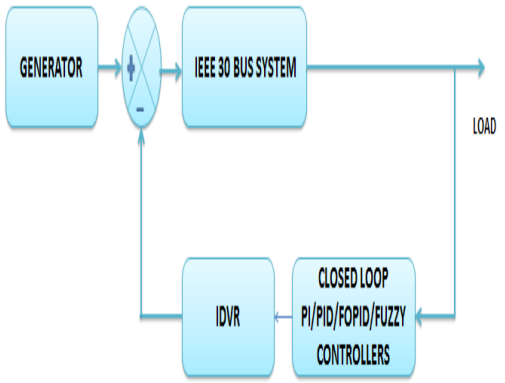

Figure 3. Block Diagram of Proposed Method.

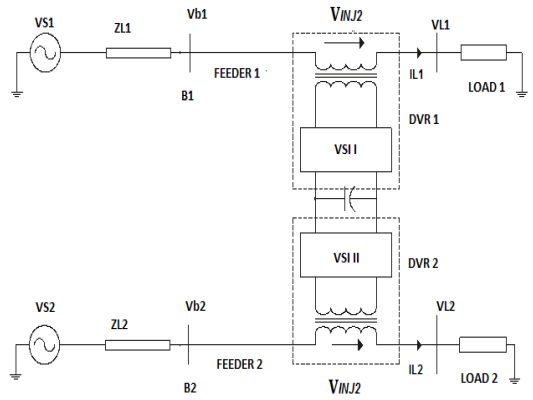

Figure 4. Circuit Diagram of Interline Dynamic Voltage Restorer.

3. Design of PI, PID, FOPID and FUZZY logic controller

In this chapter PI, PID, FOPID and FUZZY logic controller is designed. Figure 5 to 8 describe pictorial block diagram of closed loop controllers. Adjustment of input and output of Fuzzy logic rule viewer and membership function is displayed in Figure 9 and Figure 10. Obtained surface viewer for the designed fuzzy logic rule is displayed in Figure 11.

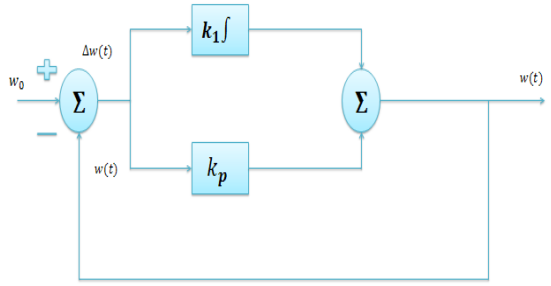

Figure 5. PI Controller.

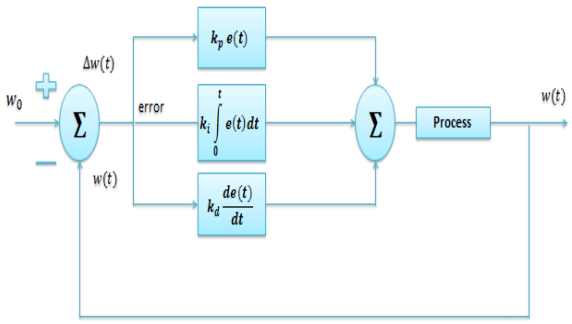

Figure 6. PID Controller.

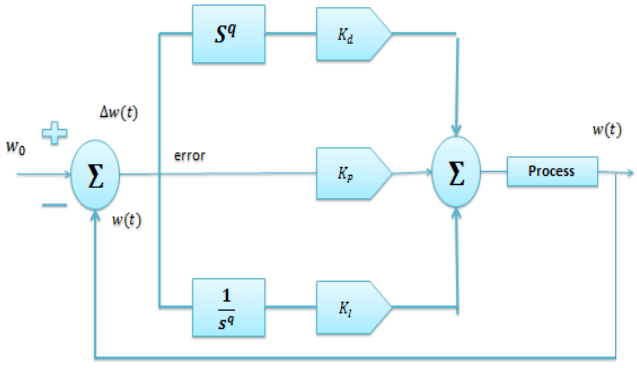

Figure 7. FOPID Controller.

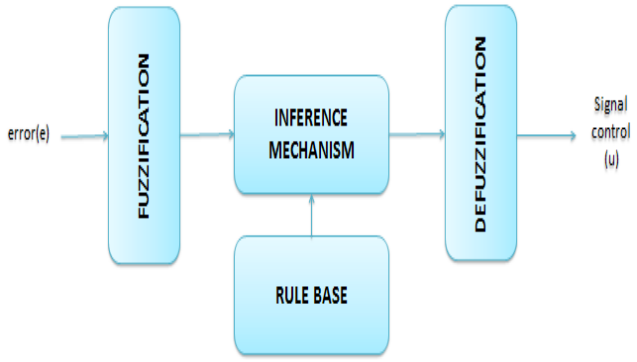

Figure 8. FUZZY Controller.

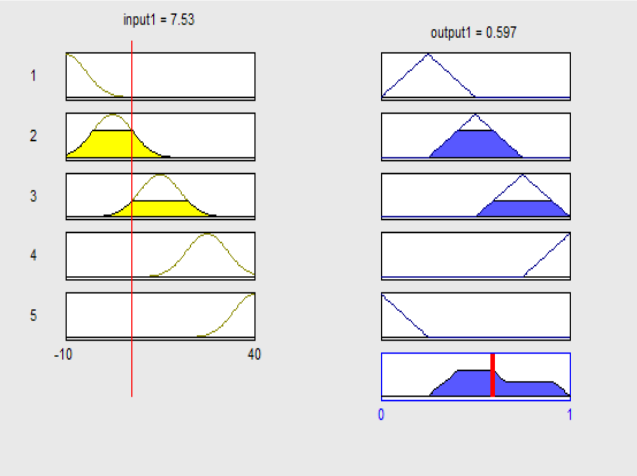

Figure 9. FUZZY Rule Viewer.

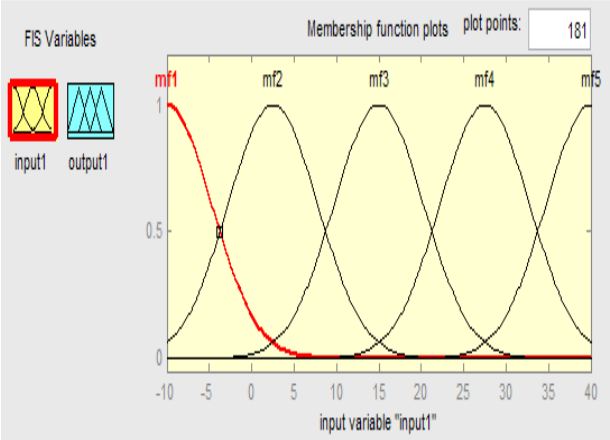

Figure 10. Fuzzy Membership Function.

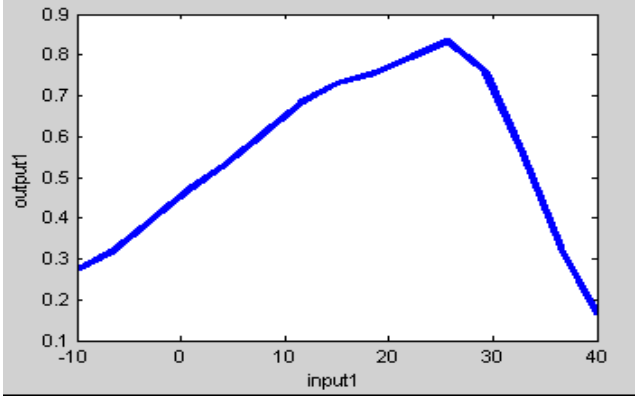

Figure 11. FUZZY Surface Viewer.

3.1 PI Controller

Proportional gain (KP) =0.1
Integral gain ki=1
Output limits= [1e6 -1e6]
Output initial value=0
Sample time=50e-6

3.2 PID Controller

Proportional gain (KP): 0.018
Integral gain (Ki): 5
Derivative gain (Kd): 0.09
Time constant for derivative (s): 0.08
Output limits: [Upper Lower] [100 -100]
Output initial value: 0
Sample time: 0.5

3.3 FOPID Controller

Proportional gain (Kp): 0.0000009
Integral gain (Ki): 0.9
Derivative gain (Kd): 0.0001
Time constant for derivative (s): 0.001
Output limits: [Upper Lower]: [1e6 -1e6]
Output initial value: 0
Sample time: 20e-6

3.4 FUZZY Logic Controller

4. Simulation Results and discussion

This chapter describes the simulation results of various closed loop control strategies such as PI, PID, FOPID and FUZZY logic controller. Voltage sag is developed in IEEE thirty bus distributed system in bus no 15 due to the addition of extra load. The desired RMS output voltage is given has feedback to the error detector and it is compared with the reference input voltage to be controlled through above controller. The error detector signal is applied to the controller, controls the duty cycle of IDVR switches inject the reactive power in distributed line and achieves the approximate desired output voltage. Simulink model has been simulated for IEEE 30 bus with IDVR system with different controllers is shown in Figure 12 and 13 respectively. Figure 14 and Figure 15 depict the output voltage, RMS voltage, Real power and Reactive power of different controllers. The time domain specifications of different controllers are represented graphically in bar chart and pie chart respectively in Figure 16 to 19. The summary of closed loop controllers results are tabulated in Table 1.

Table 1. Summary of PI, PID, FOPID, FUZZY Logic Controller

Controllers	Tr	Tp	Ts	Ess (V)
PI	0.34	0.36	0.42	4.53
PID	0.33	0.34	0.37	3.65
FOPID	0.32	0.33	0.35	2.08
FLC	0.31	0.31	0.32	0.08

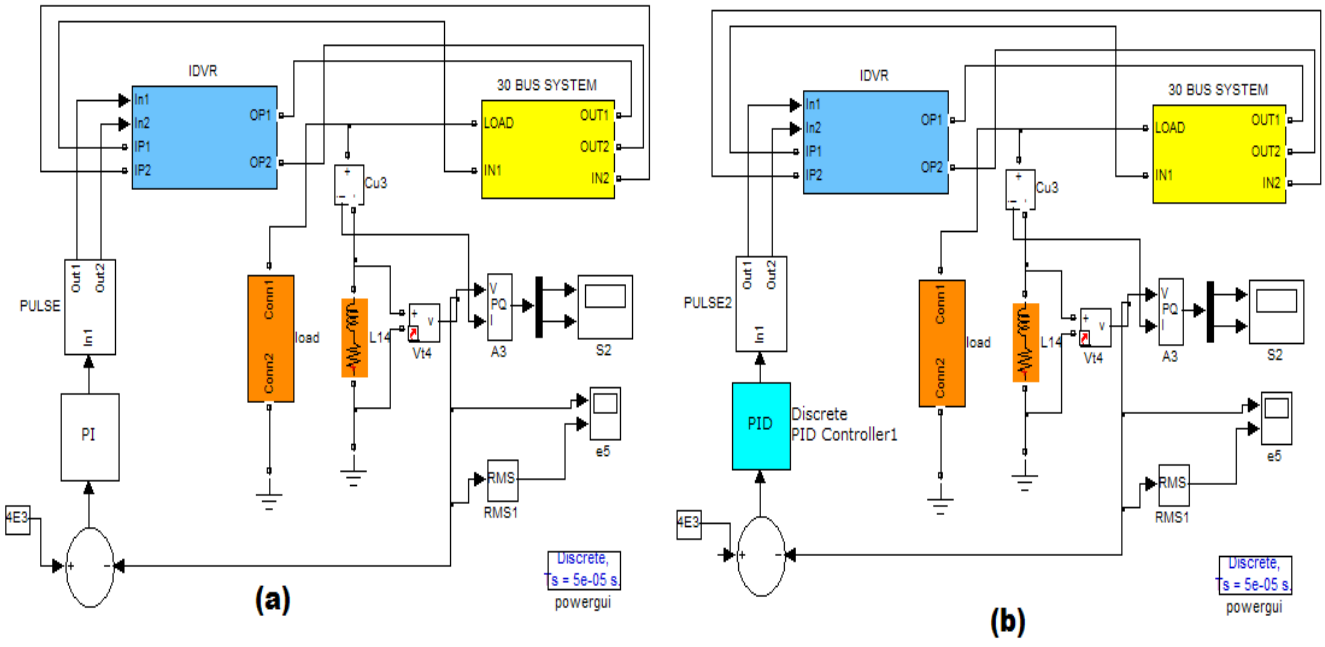

Figure 12. Simulink Model of (a) PI Controlled IDVR (b) PID Controlled IDVR.

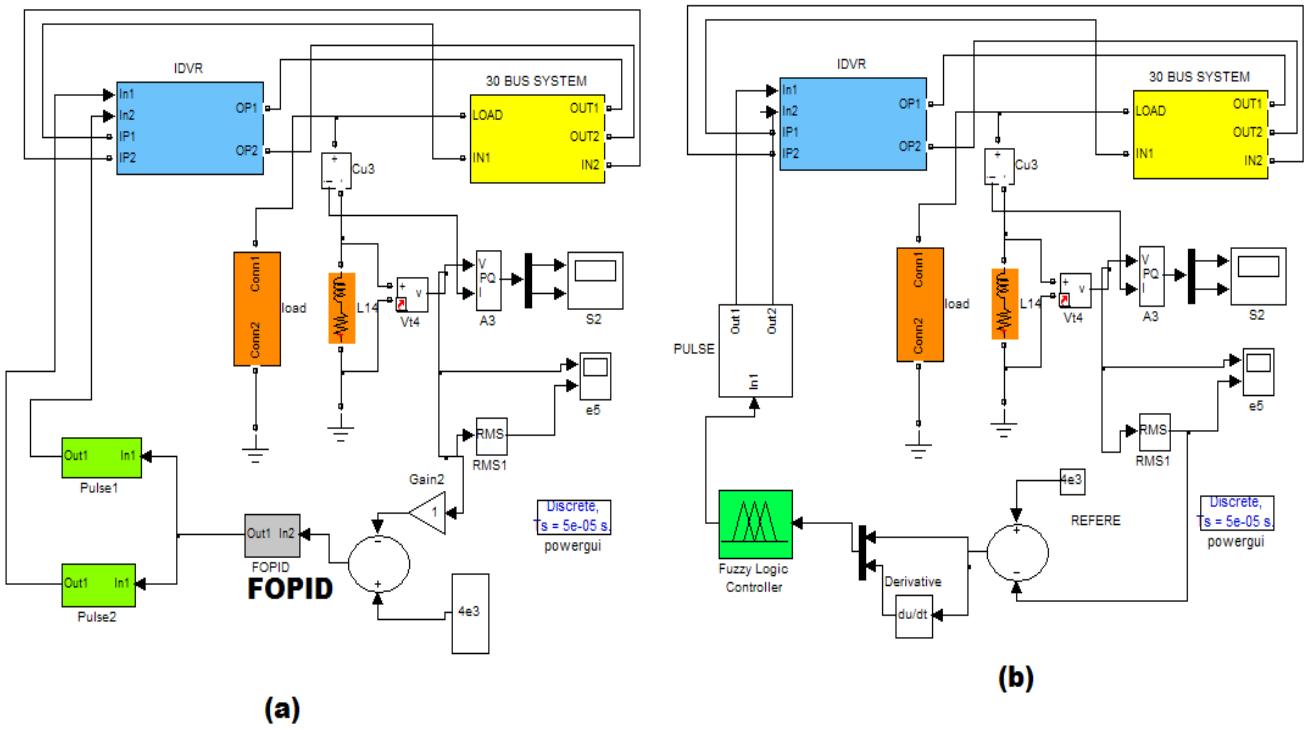

Figure 13. Simulink Model of (a) FOPID Controlled with IDVR (b) FUZZY Logic Controlled IDVR.

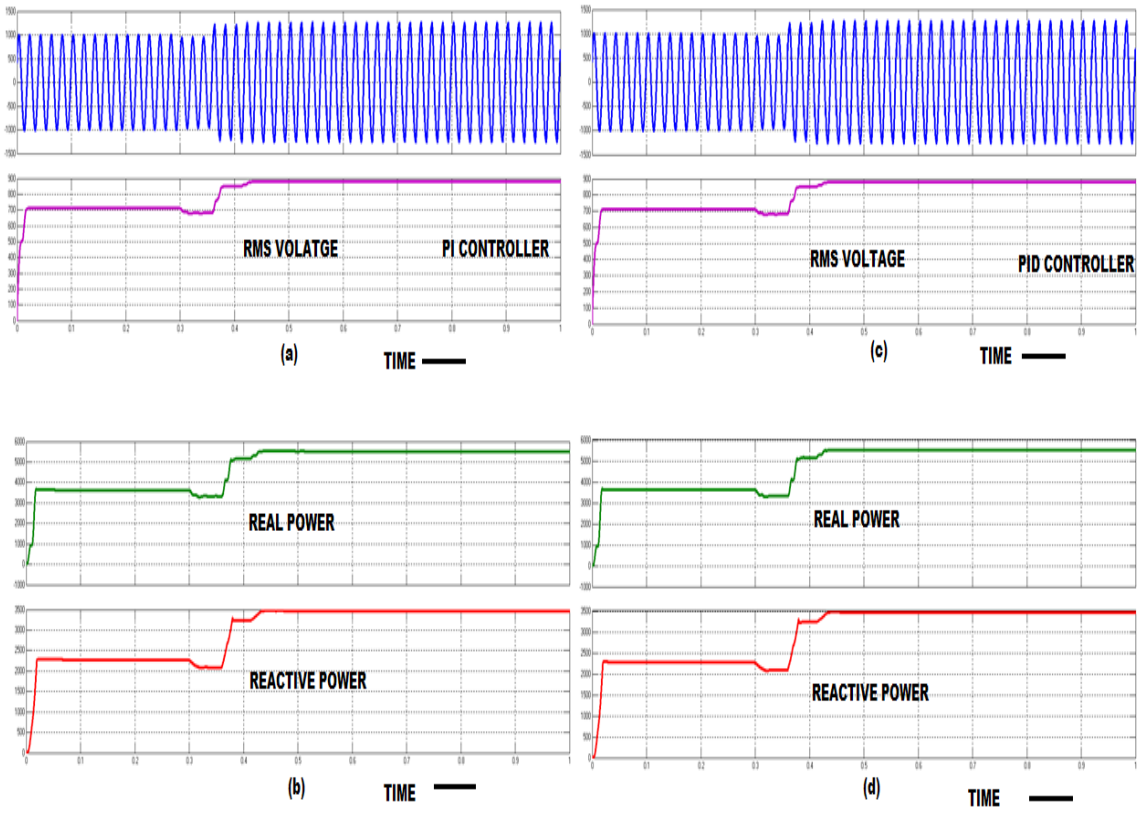

Figure 14. Simulation Output of PI and PID Controller.

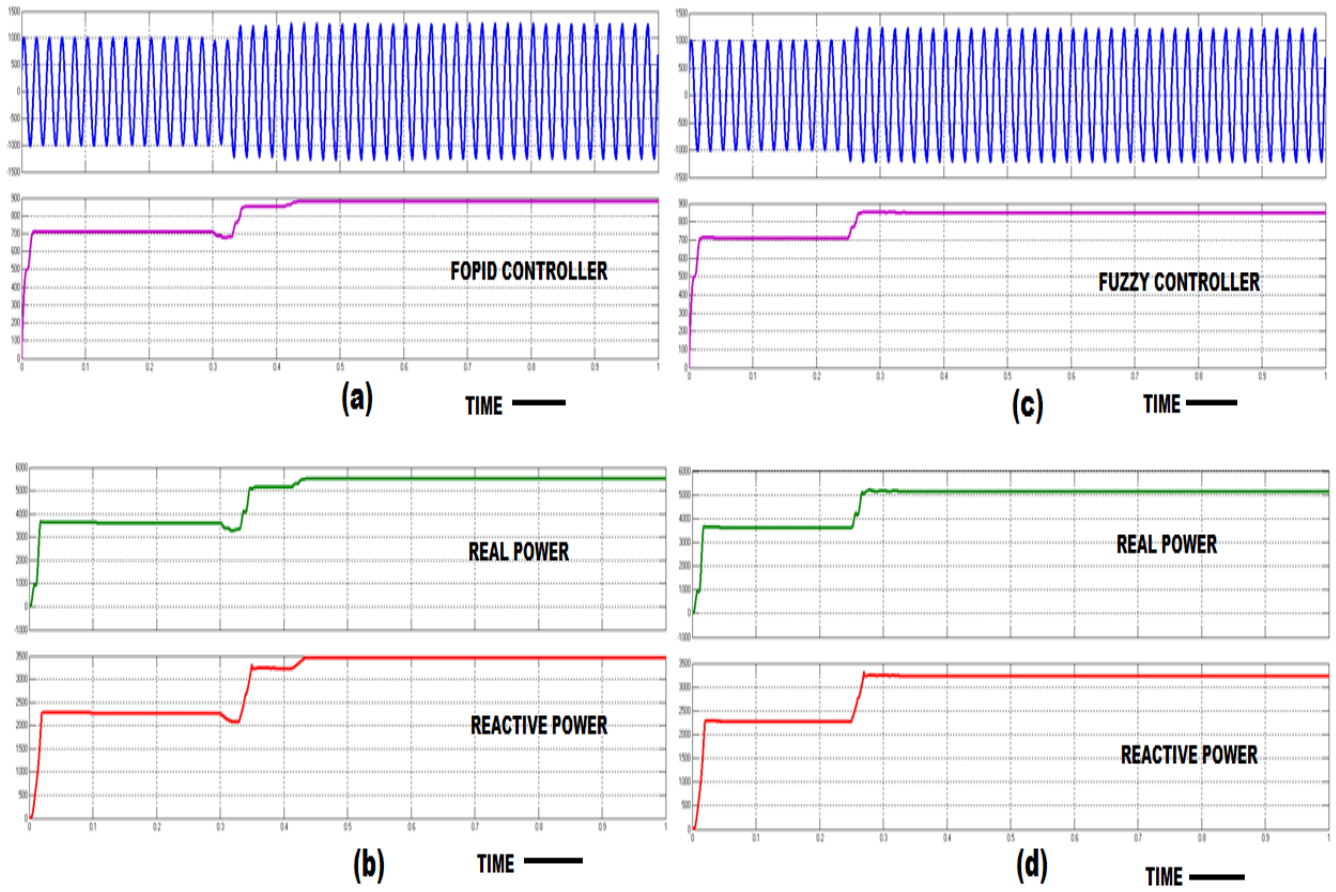

Figure 15. Simulation Output of FOPID and FUZZY Controller.

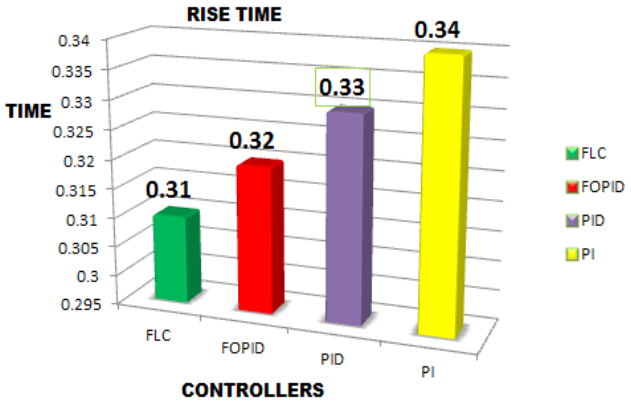

Figure 16. Summary of Rise Time.

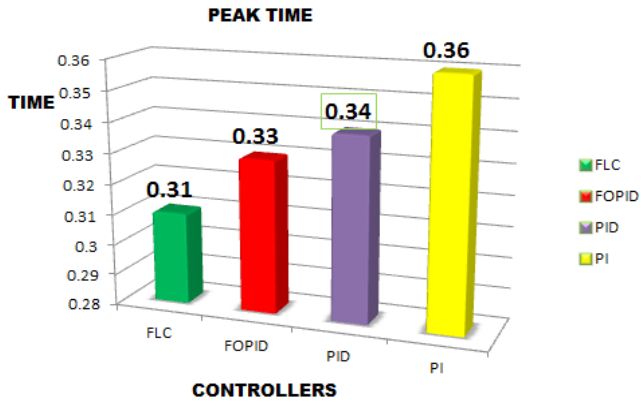

Figure 17. Summary of Peak Time.

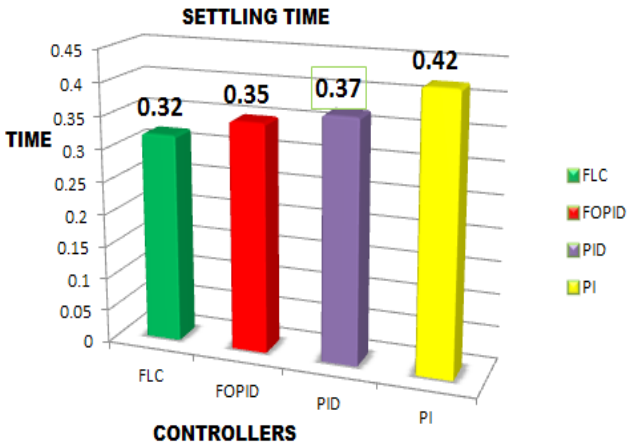

Figure 18. Summary of Settling Time.

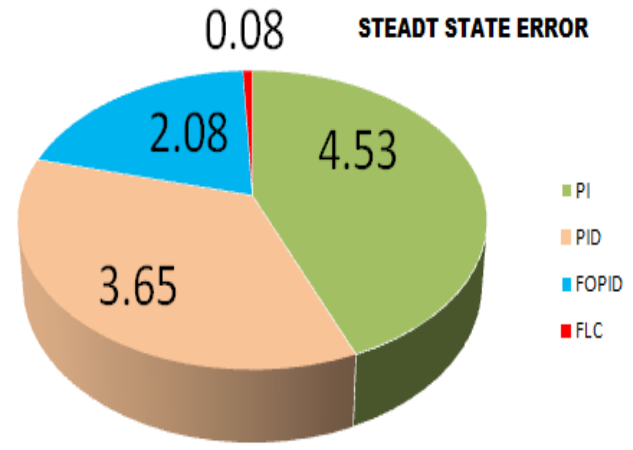

Figure 19. Summary of Steady State Error.

5. Conclusion

The results of IEEE 30 bus IDVR system is designed and simulated with PI, PID, FOPID and FUZZY logic controllers using MATLAB/SIMULINK. From the results it is known that dynamic performance of FUZZY logic controller is best in comparison to alternative controllers. The steady state error of IEEE thirty bus IDVR systems with FUZZY logic controller is found to be 0.08 sec (57% less in comparison to proportional integrated controller). Voltage profile and power transfer capability is improved in IEEE 30 bus IDVR system. Future work will be investigated in IEEE 118 bus IDVR system to further improve the voltage profile and dynamic performance.

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