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Performance Analysis of Emerging Interconnects Driven by Devices beyond CMOS

S. M. Turkane[1,2*] G. K. Kharate[1] and A. K. Kureshi[3]

[1]Matoshri College of Engineering and Research Centre, Savitribai Phule Pune University, Nashik – 422105, Maharashtra, India; satish_turkane@yahoo.co.in, gkkharate@rediffmail.com
[2]Pravara Rural Engineering College, Savitribai Phule Pune University, Ahmednagar – 413736, Maharashtra, India
[3]Vishwabharti Academy's College of Engineering, Savitribai Phule Pune University, Ahmednagar – 414201, Maharashtra, India; akkureshi@rediffmail.com

Abstract

Objective: This paper analyses the performances of Multi Walled Carbon Nanotube (MWCNT), Mixed CNT Bundle (MCB), and Multilayer Graphene Nanoribbon (MLGNR) interconnects incorporated with Carbon Nanotube Field-Effect Transistor (CNFET) and Tunnel Field-Effect Transistor (TFET) technologies. **Methods/Statistical Analysis:** The performances of the circuits are evaluated at the 32-nm node. HSPICE is used for the simulation of the driver interconnect load framework. The performance parameters, viz. power dissipation, propagation delay, and power delay product (PDP), are assessed, and it is found that a CNFET driver can reduce the propagation delay in MLGNR interconnects by 96%, 38%, and 30%, for local, intermediate, and global interconnect lengths, respectively, in comparison with the TFET driver. **Findings:** By using a TFET driver, the power dissipation in MLGNR is reduced by 99%, 45%, and 63%, for local, intermediate, and global levels, respectively, compared to the CNFET driver. The PDP of MLGNR is reduced by 99%, 37%, and 47% for local, intermediate, and global levels, respectively, by using a TFET driver instead of a CNFET driver. **Applications/Improvements:** MLGNR shows lesser propagation delay, power dissipation, and PDP than the MWCNT and MCB interconnects; hence, it is considered the best candidate to replace Cu interconnects in Very-Large-Scale Integration (VLSI) chips.

Keywords: Copper, Driver Interconnect Load. Integrated Circuits, Mixed CNT Bundle, Multilevel Graphene Nano Ribbon, Multiwalled Carbon Nanotubes, Power Delay Product, Tunnel Field Effect Transistor, Very-Large-Scale-Integration

1. Introduction

The miniaturization of Integrated Circuits (ICs) into the nanometer scale creates certain problems with respect to Cu interconnects, mainly due to the precarious increment in the resistivity of Cu, the grain-boundary scattering, and the surface scattering [1,2]. The increase in the electrical resistance within the IC interconnects may lead to a large propagation delay, which is a signal-integrity issue. This increase in the parasitic resistance of Cu interconnects presents challenges during interconnection, especially for longer lengths. Therefore, we need to look for materials other than Cu for use in interconnect applications.

As mentioned in[3,4] carbon-based materials are the most promising alternatives to Cu interconnect technology. Carbon nanotubes (CNTs) demonstrate better ballistic transport and more substantial current-carrying capacity than Cu, without electromigration issues. In contrast to Cu, CNTs demonstrate substantial mean free paths, greater electrical conductivity, and better thermal conduction[1,5]. The melting points of graphene nanostructures are quite high, compared to those of Cu; hence, the graphene nanostructures are reliable at high temperatures. The resistance and capacitance values of the interconnect affect the performance parameters of the interconnect, related to propagation delay and power

* *Author for correspondence*

consumption. Despite the improvement in the Resistance–Capacitance (RC) delay effects of the transistors with each node, the junction leakage, gate-induced drain leakage, subthreshold channel current, and gate tunnel currents are becoming increasingly significant as the dimensions of CMOS decrease[4]. To limit these, we need to look beyond CMOS device technology. Various technologies have been developed in the post-CMOS era, such as the Carbon Nanotube Field-Effect Transistor (CNFET) and the Tunnel FET (TFET). Each of these competitors, however, continues to suffer from the restrictions imposed by the interconnects. In this context, a research on the connections of interconnects with these emerging devices is essential to achieve the best circuit performance in the nanoscale regime [6]. This paper analyses the performances of Multilayer Graphene Nanoribbons (MLGNRs), mixed CNT bundles (MCBs), and Multiwalled Carbon Nanotubes (MWCNTs), and incorporated with CNFET and TFET drivers, at the 32-nm node. HSPICE is used for simulating the interconnects. Section 2 presents a simulation of the circuit, using a Driver Interconnect Load (DIL) structure, and briefly discusses the performances of MWCNT, MCB, and MLGNR with respect to power dissipation, Power Delay Product (PDP), and propagation delay. Section 3 investigates the results and delineates the fundamental augmentations. Finally, Section 4 presents the conclusions.

2. Simulation

In this section, we present here an interconnect and transistor model which are used in the simulation. We use a circuit-compatible CNFET model from the Stanford University [7] and the universal TFET model. In addition, we utilize the equivalent RLC circuit models for the MWCNT depicted in [8], MCB in [9], and MLGNR in[10]. The RLC parameters of the CNT are extracted from the CNT interconnect analyzer, and the graphene interconnect tool is used for extracting the RLC parameters of MLGNR [11]. The interconnect geometry parameters available in [12] are considered for the 32-nm node.

We use the HSPICE software, which is an analog circuit simulator, to evaluate the performances of the interconnect circuits [13]. The DIL system shown in Figure 1 is used for the performance evaluation of the MWCNT, MCB, and MLGNR interconnects incorporated with CNFET and TFET drivers, for the 32-nm node at a frequency of 0.1 GHz and load capacitance of 1 fF. The width/length ratio of the TFET is (N: P) (1:1.6) for local lengths, (30:48) for intermediate lengths, and (50:80) for global lengths. Similarly, for CNFET, the ratio of the numbers of CNTs used is (N: P) (30:30) for local lengths, (120:120) for intermediate lengths, and (240:240) for global lengths.

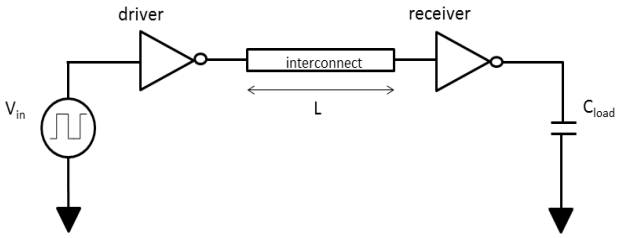

Figure 1. Test bench for simulation.

2.1 Performance Analysis with Respect to Propagation Delay

The performance of interconnect is highly affected by the propagation delay, which we cannot neglect. The propagation delays for local lengths, intermediate lengths, and global lengths are shown in Figure 2, Figure 3, and Figure 4, respectively. In these Figures, we can observe that the MLGNR interconnect demonstrates the lowest delay because the MLGNR interconnects have low RLC values compared to MWCNT and MCB interconnects. The propagation delay of CNTs can be optimized by inserting repeaters at particular intervals [14]. However, for the MWCNT interconnects, the selection of an optimum repeater depends on the impact of the contact resistance. It is observed in these Figures that the CNFET driver has a much lower delay compared to the TFET driver.

The Ge/Si Heterojunction hetero-gate dielectric with hetero-dielectric BOX PNPN TFET structure is shown in Figure 1 Technology Computer Aided Design (TCAD) is an intense tool for 2D/3D simulation of devices. A device design can be optimized for decreasing the design costs, enhancing the device design efficiency and getting the better device and the technology designs. The simulation is helpful in predicting the electrical characteristics of devices. We have used a Kane Band-to-Band Tunneling model in which value of two parameters of Kane's model are A.BTBT = 3.9e+22eV $^{(-1/2)}$ $cm^{-1}s^{-1}V^{-2}$ and B.BTBT = 2.25e+07 $Vcm^{-1}eV^{(-2/3)}$. Also a mobility model like Lombardi mobility model is used.

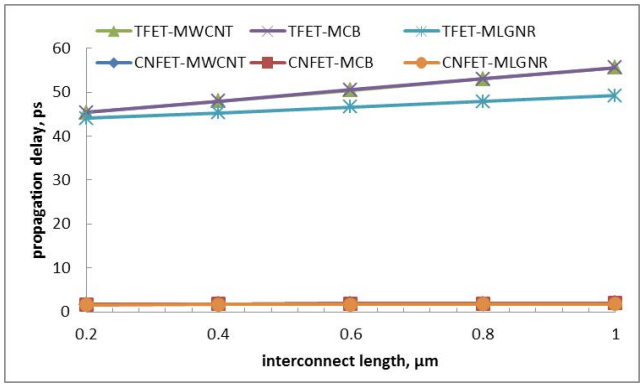

Figure 2. Propagation delay for local interconnects.

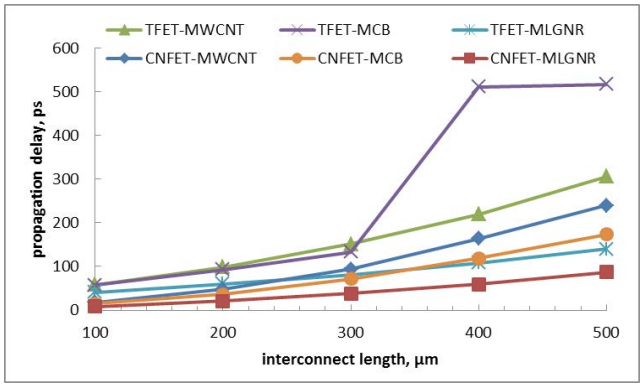

Figure 3. Propagation delay for intermediate interconnects.

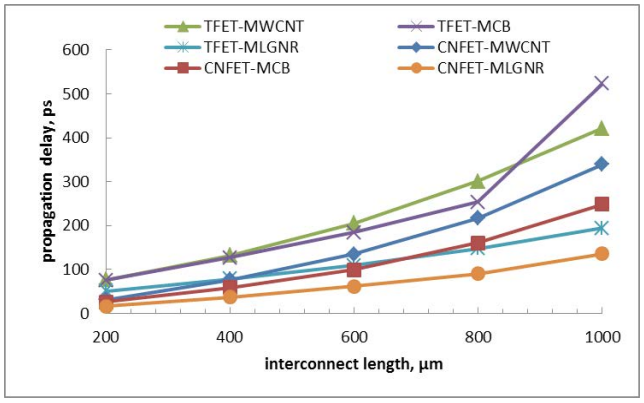

Figure 4. Propagation delay for global interconnects.

2.2 Performance Analysis with Respect to Power Dissipation

Power dissipation is an important parameter, which affects the performance of a system. The power dissipation of an ideal system must be low. We analyze the power dissipations of the MWCNT, MCB, and MLGNR interconnects for various interconnect lengths, as shown in Figure 5, Figure 6, and Figure 7. From the Figures, it can be observed that, when a TFET driver is utilized, the power dissipation remains very low compared to when a CNFET driver is utilized. Among all combinations, TFET–MLGNR exhibits the lowest power dissipation.

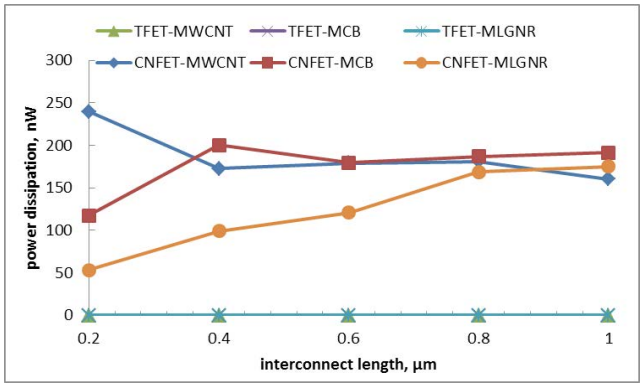

Figure 5. Power dissipation for local interconnects.

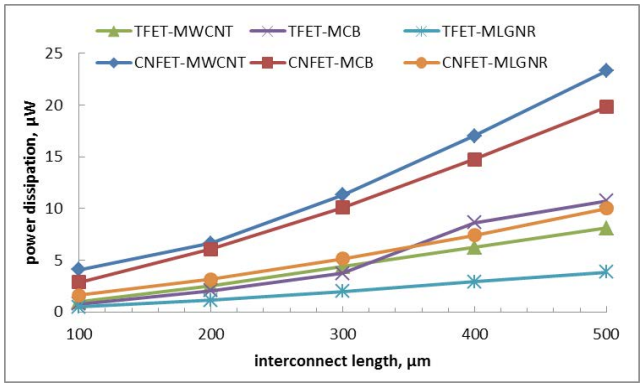

Figure 6. Power dissipation for intermediate interconnects.

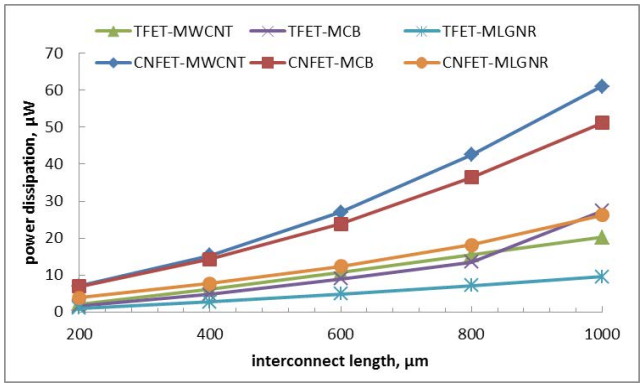

Figure 7. Power dissipation for global interconnects.

2.3 Performance Analysis with Respect to Power Delay Product

The PDP is a combination of the propagation delay and

power dissipation, and provides the amount of power consumed for an observed delay. We calculate the PDPs for MCB, MWCNT, and MLGNR interconnects, as shown in Figure 8, Figure 9, and Figure 10, for various interconnect lengths. As the TFET driver provides extremely low power consumption, the PDP of the TFET driver remains very low compared to that of the CNFET driver.

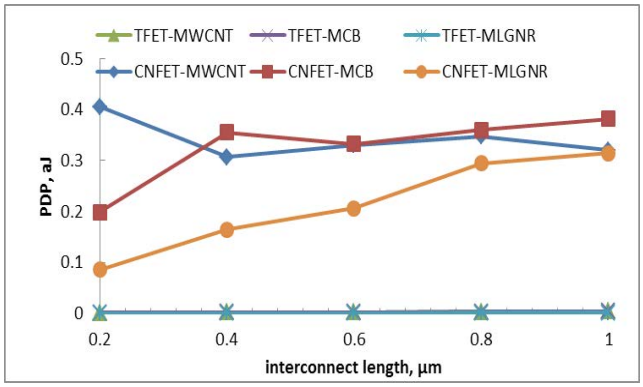

Figure 8. PDP for local interconnects.

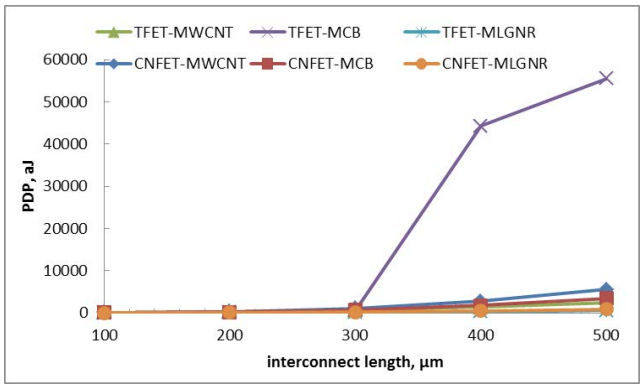

Figure 9. PDP for intermediate interconnects.

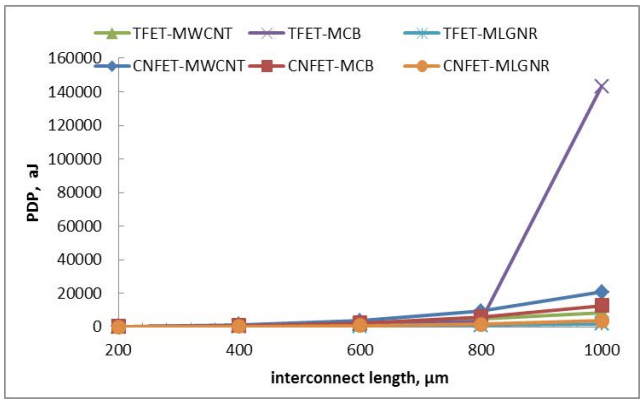

Figure 10. PDP for global interconnects.

3. Results and Discussion

After simulating a test bench, the propagation delay and power dissipation were extracted for various lengths, as shown in Table 1 and Table 2, respectively. For smaller lengths, the delay was very short; however, as the interconnect wire length increased, the delay also increased. As the CNFET transistor has a high current-driving capacity, the CNFET driver provides a shorter propagation delay.

When we compared the propagation delays of the local interconnects utilizing the CNFET and TFET drivers, we found that the delay in the CNFET-incorporated devices was 96% less than the delay in the TFET-incorporated devices.

At the intermediate level, the propagation delay was reduced by 21% in the CNFET–MWCNT interconnect, 66% in the CNFET–MCB interconnect, and 38% in the CNFET–MLGNR interconnect, compared to the TFET–MWCNT, TFET–MCB, and TFET–MLGNR interconnects, respectively.

Similarly, at the global level, we found propagation-delay reductions of 19% in the CNFET–MWCNT interconnect, 52% in the CNFET–MCB interconnect, and 30% in the CNFET–MLGNR interconnect, compared to the TFET–MWCNT, TFET–MCB, and TFET–MLGNR interconnects, respectively.

When we compared the power dissipations in the interconnects utilizing the CNFET and TFET drivers, we found 99% reduction in the TFET–MWCNT, TFET–MCB, and TFET–MLGNR interconnects, compared to the CNFET–MWCNT, CNFET–MCB, and CNFET–MLGNR interconnects, respectively, at the local level. At the intermediate level, 65% reduction in the TFET–MWCNT interconnect, 45% reduction in the TFET–MCB interconnect, and 45% reduction in the TFET–MLGNR interconnect were observed, compared to the CNFET–MWCNT, CNFET–MCB, and CNFET–MLGNR interconnects, respectively. At the global level, 66% reduction in the CNFET–MWCNT interconnect, 46% reduction in the CNFET–MCB interconnect, and 63% reduction in the CNFET–MLGNR interconnect were observed, compared to the TFET–MWCNT, TFET–MCB, and TFET–MLGNR interconnects, respectively. We found 99% reduction in the PDP at the local level, 37% reduction at the intermediate level, and 47% reduction at the global level for TFET–MLGNRs, when compared to the CNFET–MLGNRs.

Table 1. Propagation delays for various interconnect lengths at the 32-nm node

Wire length (μm)	Propagation Delay (ps)					
	CNFET			*TFET*		
	MWCNT	*MCB*	MLGNR	MWCNT	MCB	MLGNR
Local						
0.2	1.6937	1.6945	1.6142	45.346	45.353	44.043
0.4	1.7749	1.7762	1.6611	47.908	47.923	45.322
0.6	1.8481	1.8512	1.7068	50.467	50.489	46.612
0.8	1.9204	1.9225	1.7503	53.016	53.045	47.895
1	1.9934	1.9963	1.7939	55.551	55.587	49.176
Intermediate						
100	17.512	14.573	8.7011	58.485	57.556	41.105
200	47.308	36.039	20.526	98.591	92.635	59.974
300	93.402	71.352	38.136	150.89	133.35	81.563
400	163.77	118.37	59.336	219.76	511.81	107.75
500	239.34	173.24	86.521	305.91	517.07	139.76
Global						
200	31.177	26.24	16.045	75.963	75.751	50.451
400	76.092	58.282	36.836	132.10	127.06	78.051
600	134.59	99.28	61.612	204.98	184.44	109.12
800	217.18	160.62	89.993	300.59	253.48	147.23
1000	339.46	247.97	135.67	421.28	523.28	194.00

Table 2. Power dissipations for various interconnect lengths at the 32-nm node

Wire length (μm)	Power Dissipation					
	CNFET			*TFET*		
	MWCNT	*MCB*	MLGNR	MWCNT	MCB	MLGNR
Local (nW)						
0.2	239.74	117.53	53.337	0.03371	0.03352	0.003120
0.4	172.67	200.22	99.353	0.04273	0.04222	0.008771
0.6	179.09	179.75	120.87	0.05175	0.05088	0.013123
0.8	181.08	187.08	168.53	0.06057	0.05926	0.019919
1	160.51	191.48	175.26	0.06909	0.06742	0.027867
Intermediate (μW)						
100	4.1027	2.8632	1.6301	0.97279	0.77344	0.4594
200	6.6355	6.0757	3.1509	2.5454	2.0632	1.1427
300	11.304	10.073	5.1507	4.3528	3.7102	1.9958
400	17.012	14.745	7.4181	6.2225	8.6456	2.9135
500	23.315	19.819	10.011	8.1063	10.741	3.8507
Global (μW)						
200	7.0633	6.9399	3.8882	2.1346	1.5932	0.9835
400	15.276	14.302	7.6409	6.0707	4.7773	2.7171
600	26.999	23.848	12.331	10.614	8.9071	4.8722
800	42.562	36.375	18.102	15.363	13.448	7.1792
1000	61.078	51.219	26.156	20.162	27.351	9.5642

4. Conclusion

The performance parameters of MCB, MWCNT, and MLGNR interconnects utilizing CNFET and TFET drivers were analyzed for different interconnect lengths. MLGNR interconnects demonstrated lower power dissipations, shorter propagation delays, and lesser PDPs, compared to MWCNT and MCB interconnects. A CNFET driver exhibited less propagation delays in interconnects, than the TFET drivers. Whereas, TFET drivers provided very less power dissipation in interconnects, compared to the CNFET drivers. Thus, TFET drivers provided lesser PDPs than the CNFET drivers. Therefore, it could be inferred that CNFET can provide better performance for applications where speed is critical. Similarly, for low-power applications, TFET

drivers can provide lower power consumptions. In terms of PDP, interconnects incorporated with TFET drivers provide better performances than those incorporated with CNFET drivers. Thus, TFET drivers are considered much better for low-power moderate-speed applications, whereas CNFET drivers will be the best options for high-speed applications. Research is being conducted for determining the life span, durability, and cost effectiveness of the emerging interconnects.

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