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A Study on Advanced High Speed and Ultra Low Power ADC Architectures

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Abstract

Background: Analog-to-digital converter (acronym as ADC) is an electronics device used to convert a continuous physical signal to a digital number. Over recent years, different advancement has been done and both the beginner as well as expert can be bewildered to differentiate their limitations and benefits. **Objective:** To overcome this problem this paper provides a brief study about these advance architectures and their parameters. The deliberation of these parameters can make a suitable decision to adopt a better architecture for the purpose of research. **Methods:** reviewed in this paper include parametric and non parametric ultra low, high speed, low noise architectures.

Keywords: ADC Architectures, SAR DAC, TI ADC, PWM ADC

1. Introduction

Usually all the information available in the world is in the form analog data. Although accumulating the analog data in the memory is more arduous than digital data storage. It can be anticipated that digital data requires less memory to get store and can be efficiently and effortlessly encrypted for security reasons. So, there is requirement of Analog to Digital Converter (ADC) for its useful purpose in digital signal processing. ADC is only applicable in all electronics systems because there the data required is in the form of digital data. There is need of ultra low voltage ADC that consumes least power for the conversion. For example our function is in the form of cosine wave. Figure 1 shows the transformation of digital signal from analog signal.

The conversion shown in Figure 1 involves conversion of continuous Sin wave to digital value with the help of quantization, so it definitely gives some error. There are a number of energy constrained electronic gadgets such as mobile phones and sensors etc requiring adequate power ADCs. For the time being, to attain the goal of power efficient ADCs, the hardware complexity must not increase considerably. SAR ADC is generally a very dominating architecture because of its power efficiency and digital virtues. In previous years, various techniques has been presented to increase the speed of Successive Approximation Register ADC and also, to minimize their power consumption. However, decreasing the supply voltage is decisive method for achieving this but at near threshold values, these results in higher distortion and lower bandwidth.

There is also another type of ADC which is delta sigma ($\Delta\Sigma$) ADC. Although in the delta sigma type ADC a common concept for all is present known as, oversampling. Oversampling means to take many samples of analog signal and to calculate the average of digitized signal. At the end, there is an effective increase in number

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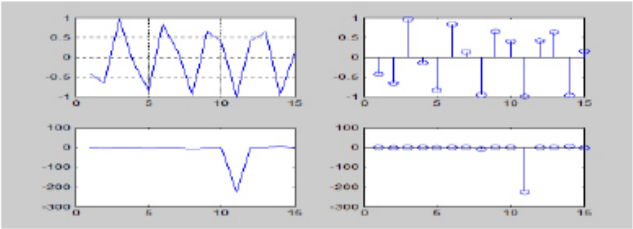


Figure 1. Khatak: transformation of digital signal from analog signal.

of bits resolved in signal. In short, one bit ADC can do the same work as 8-bit but at slow rate means time complexity increases to do a job. There is another type known as FLASH ADC. Such types of converter are assumed to be very ideal for those applications which acquire large bandwidth. Though there is a limitation of flash ADC that they consume more power.

Most of the modern data converters operate less than 1V single supply. There is a rapid growth in demand of +3V electronic devices like mobile phones, digital cameras etc. In case, lower supply voltages are used for smaller input voltage ranges, and there will be much more sensitivity towards noise from all sources and references. Sensitivity towards noise or error can be caused by decoupling techniques, etc[1]. Single-supply ADCs often have an input range which is not referenced to ground. Finding compatible single-supply drive amplifiers and dealing with level shifting of the input signal in direct-coupled applications also becomes a challenge.

2. ADC Parameters

There are many ADC parameters which decide the ADC performance. Some of the parameters are:

2.1 Resolution

Resolution is generally represented in bits. Resolution in an ADC device can be function of dividing a maximum signal into parts. The best resolution in ADC is one part from $2n$ where n is the number of bits of ADC. So lower the resolution more accuracy will be gained. For example, if we take a 10 bit ADC then its resolution will be $\frac{1}{2^{10}}$.

2.2 Signal to Noise Ratio (SNR)

This is most important ADC parameter. It is the ratio of power of the essential information called signal power of the unwanted signal called noise for the output signal and measures the amount of signal distorted. It is generally represented in decibels (dB). To represent in decibels we just have to multiply the calculated SNR with $10log_{10}$.

2.3 Power Consumption

It gives amount of power dissipated by an ADC. It generally depends on circuit area. Less is the circuit area, less will be power dissipation.

2.4 Nyquist Sampling Rate

It gives the lower bound for the alias free sampling. The largest frequency of the low pass signal or band pass signal must be less than the sampling frequency.

$$f_n < {}^{f_k}/_{2}$$

Where f_n is the greatest frequency and ${}^{f_k}/_{2}$ is the Nyquist frequency and $2 * f_n$ is Nyquist rate.

2.5 Figures of Merit (FOM)

FOM of ADCs suggests that adding extra bit in an ADC is difficult as doubling the bandwidth of ADC.

$$FOM = \frac{Power}{2^{ENOB}.f_s}$$

Where f_s is Nyquist Sampling Rate and, ENOB is ENOPs defined by SNR.

3. Types of ADC Architecture

Various architectures are studied during the review of various advancements of ADC architecture. Some really good and useful architecture are discussed in this section. These are as follows.

3.1 SAR ADC Architecture

SAR ADCs can be implemented in two ways one is fully differential and another is single ended[2]. Fully differential architecture has many advantages such as better noise rejection, better distortion performance, and an increased output voltage swing. It is not favoured in case of power consumption and area efficiency. Also, fully differentials ADCs may require some extra design efforts and some more power in preceding neural amplifiers. Conventional architectures involve more drawbacks other than this. Firstly, the comparator is needed to provide same range

as the input voltage. This is a challenging task especially in case of rail-to-rail input. Other drawback is the size of capacitor array. If the size of a capacitor array is halved by the use of top-plate sampling then, this will result in a potential non linearity error. Figure 2 shows the architecture of SAR DAC.

An improved architecture is proposed to address the above mentioned issues but at the cost of higher power dissipation[3].In this, a common mode buffer is introduced. The technique used in improved architecture is the auto zeroing technique. The optimal common mode voltage is set to half of the reference voltage.

3.2 TI-ADC Calibration Technique

The conventional ADCs have some time mismatch errors in them which are static in nature. TI-ADC is a calibration technique which is used to correct these types of mismatches. The technique mainly use the concept presented in the slow and an accurate reference ADC[4]. In this architecture, the sampling edge of the reference ADC matches to every Sub-ADC present there in a periodic manner. If there is a mismatch error then despite giving same input, the quantization result of both reference ADC (D_r), and the i^{th} Sub-ADC (D_i) may differ from each other. So, their variance between the two outputs helps in driving a Digital Equalizer (DE) such that transfer function of each sub-ADC gets aligned with the reference ADC and, consequently the mismatch errors can be rejected. The calibration can be outspreaded to remove all static mismatches; however dynamic errors can still be present in the system. Figure 3 shows Calibration of TI-ADC.

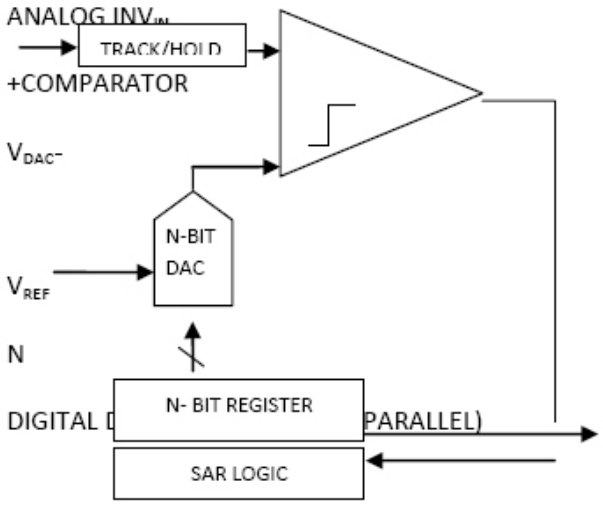


Figure 2. Khatak: Architecture of SAR DAC.

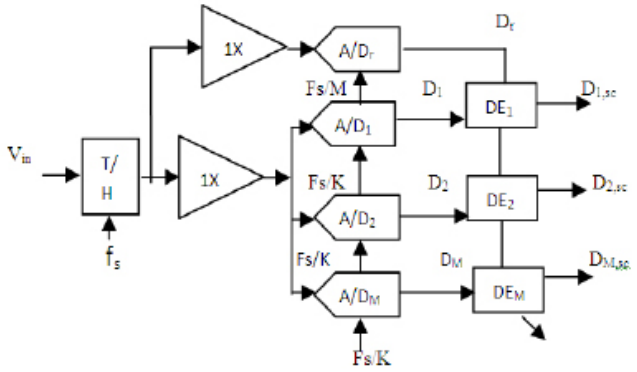


Figure 3. Khatak: Calibration of TI-ADC.

3.3 TI-ADC Skew Calibration Technique

This calibration technique which is operating on Direct Derivative Information (DDI) is a novel skew calibration. The system architecture is equivalent to the above discussed calibration with an exception of the front end S/H. The basic idea behind this is to constrain all the sub-ADCs to behave identical to the reference ADC in static transfer function and as well as in timings. Suppose the errors induced by skew are not large then, the first order expansion of the series will be

$$Dr - \mathbf{Di} = \frac{\mathbf{dv}}{\mathbf{dt}}.\mathbf{\Delta t}$$

Where, D_r and D_i are the digital outputs of reference ADC and Sub-ADC respectively, and Δt is the timing skew of i^{th} path. $\frac{dv}{dt}$ is the derivative term of input? Now, the net skew can be articulated as

$$\mathbf{\Delta}t = D - Di \Big/ \frac{dv}{dt}$$

The High Pass Filter (HPF) output is measured using an auxiliary ADC, so as to get the complete knowledge about the input derivative, which can be used in a digital domain skew error compensator. Since only sign information is essential.

A Digitally Controlled Delay Element (DCDE) is also used in the calibration to adjust the timings of sub ADC paths to make them equal to the reference ADC, in order to eradicate the skew errors. Figure 4 shows T1-ADC Skew Calibration Technique.

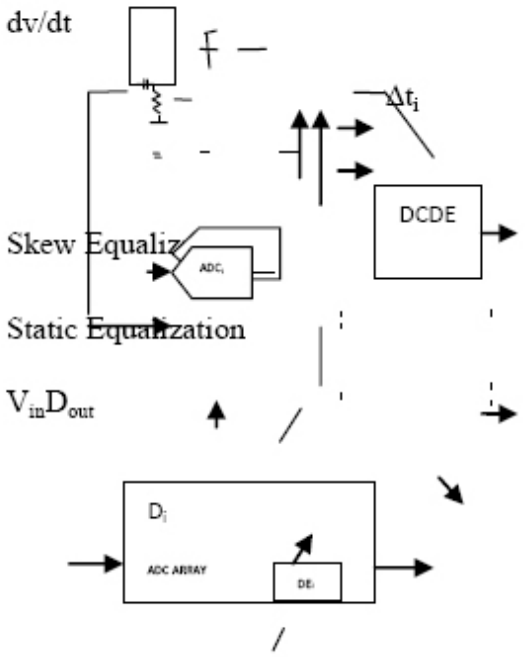


Figure 4. Khatak: T1-ADC skew calibration technique.

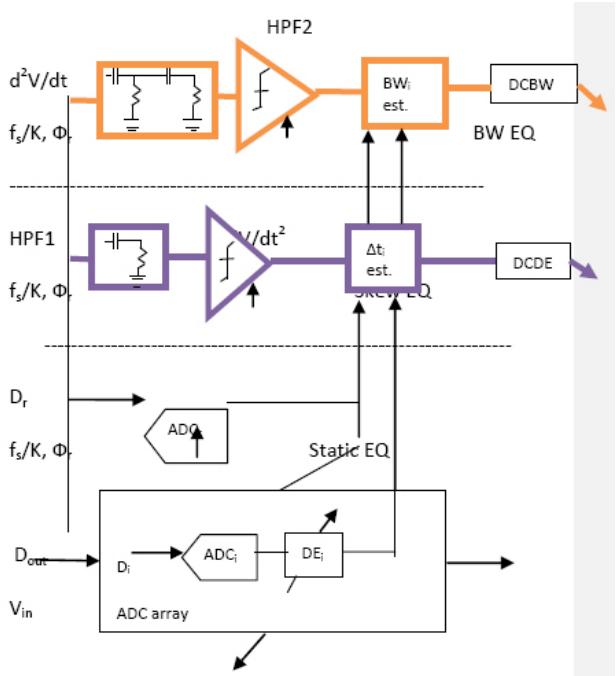


Figure 5. Khatak: TI-ADC comprehensive calibration.

3.4 TI-ADC Comprehensive Calibration

Since it is known that the skew calibration technique can not ensure the linearity of a wideband TI-ADC array in isolation when the bandwidth mismatch is also there. This architecture extends the previous architecture for the treatment of bandwidth mismatch errors along with the correction of skew errors[4]that results in comprehensive dynamic error calibration. The conventional single-pole, low pass model is used.

The architecture of this calibration is shown in Figure 5. Along with skew calibration block architecture, a first order CR HPF, a DCDE circuit a zero-crossing comparator present in the previous architecture, a bandwidth mismatch calibration block is also included which consist of a zero crossing comparator, second order CR-HPF, and S/H bandwidth adjustment circuit.

Here, two dynamic loops and a static calibration loop are included instantaneously. To comprehend second order HPF two first order ones are directly cascaded.

3.5 Interpolated Pipeline ADC Architecture

Pipelined ADC architecture is used for moderate resolution conversion and high speed. However there is an insufficient amplifier gain in scaled CMOS technologies so, to design a closed loop residue amplifiers having higher speed becomes more challenging. Therefore an alternate to this called the interpolated technique is applied in pipeline fashion[1]. Now, open loop amplifiers having simple topology are to be used for simplification which may help us to overcome supply voltage scaling problems as gain requirements are relaxed using simple amplifiers. Which are used in pipeline ADC to enhance its conversion rate?

Figure 6 shows the block diagram of this scheme. In first stage a pair of capacitor array is used to sample the input signal V_{in} and reference voltage V_{ref}. V_{in} is shifted by $+V_{ref}$ to realize interpolation. Then first set of conversion data is generated by 3-bit sub-ADC (CMP1) and capacitor arrays generate required $V_{res1,1}$ and $V_{res2,1}$ signal for next stage.

At next stage, both inputs are amplified by A1a and A1b which is then sampled on IntCaps and quantized by CMP2. At final stage 2 more amplifiers A2a and A2b with CMP3 provides final set of conversion data.

Figure 6 shows Interpolated Pipeline ADC architecture.

3.6 Power and Bandwidth Scalable SAR ADC

This technique is similar to delta sigma ADC, except the decimation filter and active loop filter, which are

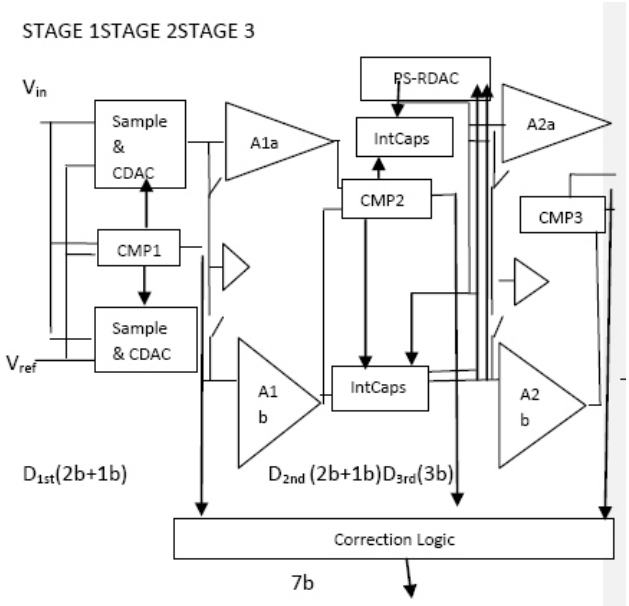


Figure 6. Khatak: Interpolated pipeline ADC architecture.

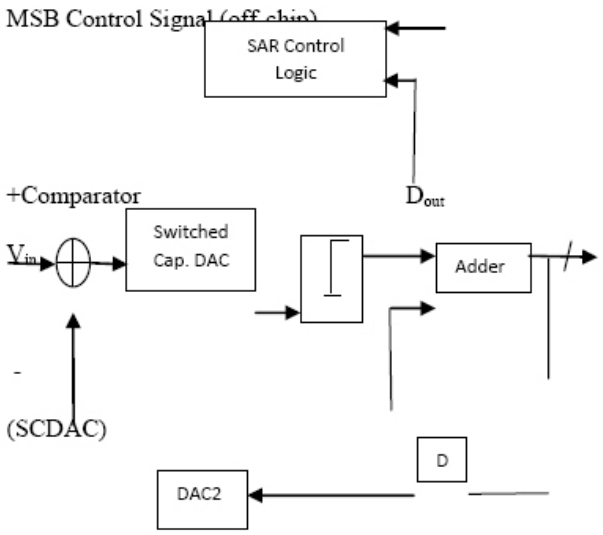


Figure 7. Khatak: SAR ADC.

much power consuming are replaced by a digital adder and passive Switched-Capacitor DAC (SCDAC)[5]. This ADC which runs on different Oversampling Ratios (OSRs).Principle of the study is that, without increasing the hardware complexity significantly, the power consumption can be reduced to an extent. Figure 7 shows SAR ADC.

3.7 Hybrid Radix-3/Radix-2 SAR ADC

This approach is SAR ADC is used with low hardware configuration. It is a hybrid approach in which both single ended Redix-3/ DifferentialRedix-2 are used[6]. Redix-3 is used for searching first few mean significant bits of and the second one finds the rest of the bits. Radix-3 search gives faster rate of convergence and requires very low-resolution. However, the Differential radix-2 search reduces the comparator offset effect with a higher resolution comparator and power.

In this technique two comparators and two capacitors are used to perform the single ended ternary search. Both the capacitors act as MSB and LSB. The LSB capacitor requires three comparison cycles to produces 4.8 bits. Differential Redix-2 search requires one capacitor and another comparator. It produces 3 bits in three comparison cycles. So in total it requires six clock cycles to produce 7.8 bit result.

H. SAR ADC with Threshold Configuring Comparators (TCC)

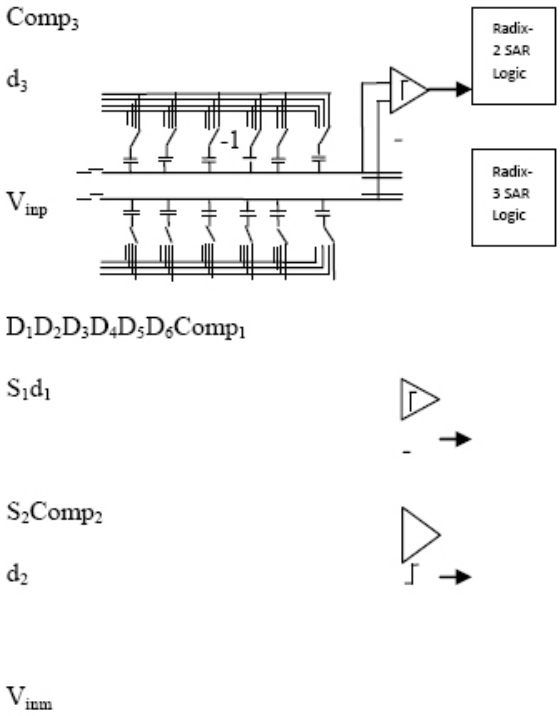


Figure 8. Khatak: Hybrid radix 3/radix 2 SAR ADC.

The conventional SAR ADC has a tailback of speed, as n cycles are required in SAR search algorithm to obtain a resolution of n bits. The 2-bit/step can increase the speed to its double without time interleaving. Although this requires three times the number of

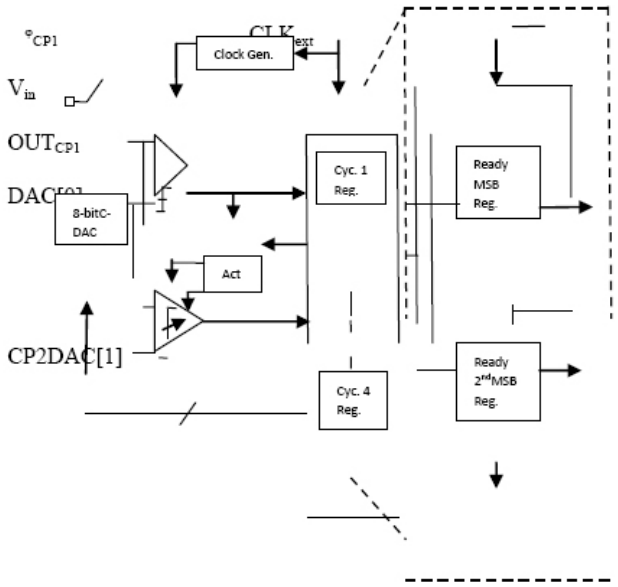
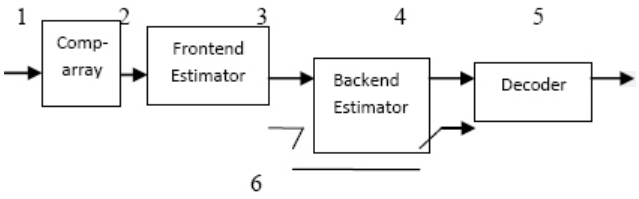


Figure 9. Khatak: SAR ADC with threshold.



1 Analog input X in range I

2 Binary observations in range I

3 Binary observations in range I_{FE}

4 N_{BE}bits

5 N bits

6 S decisions mapping to N_{FE}bits

Figure 10. Khatak: Statistical ADC block diagram.

elements in conventional SAR ADC which results in large power consumption. The method includes addition of TCC into a simple SAR ADC[3]. Although both power and area overhead are very small but there is an increment of over 50% in speed of convertor at 0.3-0.6V power supply. The threshold value of comparator is dynamically configured using variable currents. The generated V_{cm} voltage biases the Variable Current Sources (VCS) internally to make the ADC independent from voltage variations[3].

3.8 Flash Type ADC Architecture

The statistical ADC consists of mainly a comparator array, a front end estimator, a back end estimator, and decoder logic. In the optimized system the front end and back end estimators perform different but interdependent functions[7]. The precision given by the front end estimator affects the complexity and performance of back end estimator. The basic computations are simple addition over binary observations in both estimators. In front end estimator, the additions determine the ratio of 1s over Front end Clusters (FC) and in back end estimator additions determine the ratio of 1s over Back end Clusters (BC). The statistical ADC is also limited by the error probability as the traditional ADC. Figure 10 shows the block diagram of Statistical ADC.

3.9 Ultra Low Voltage Self Calibrated SAR ADC

This architecture is about self calibration SAR ADC which operates on 0.5V and producing 11bit output at a scaled frequency of 500 Ks/s[8]. Bottom plate sampling is also employed to eradicate the gain error produced by parasitic or stray capacitance. To avoid the poor matching due to fractional values, the scaling between LSB and MSB array chosen to be unit scaling capacitor. This work shows that there is significant effect of non linearity between calibration DAC and a coupling capacitor in their studies various parameters are analyzed and optimized accordingly. They have achieved a FOM between 76 and 77 (76.3) fJ/conversion step with a power supply of 39.9 μW[8]. Figure 11 shows self-calibrated ADC architecture.

K. Pulse Width Modulated (PWM) Delta-Sigma ADC

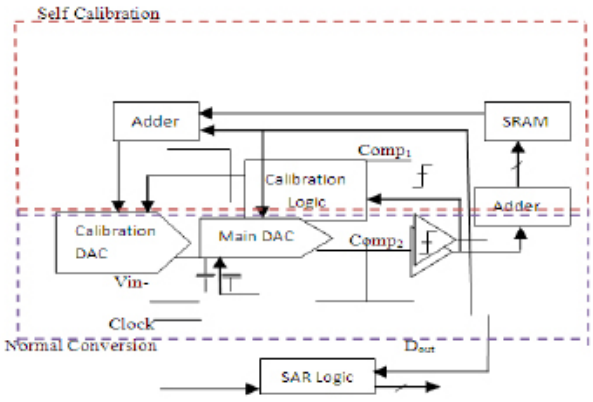


Figure 11. Khatak: Architecture of the self-calibrated ADC.

Table 1. Comparison table for various ADC architectures

	Refnc[1]	Refnc[2]	Refnc[3]	Refnc[4]	Refnc[5]	Refnc[8]	Refnc[9]	Refnc[10]	Refnc[11]	Refnc[12]
Technology	90nm	----	40nm	----	----	130nm	----	65nm	----	0.18
Architecture	Pipeline	SAR	SAR	----	SAR	SAR	Delta-Sigma	Sub-ranging	SAR	Single end SAR
Resolution (bit)	7	10	8	8	10	11	12	7	14	10
F_s[MS/s]	160	-----	----	----	30	----	----	820	----	460KS/s
SNDR[dB]	----	55.3dB	43.3dB	----	69.4dB	62.1 dB	----	37.4dB	----	90.8dB
Consumed Power	2.43mW	9mW	0.20μW	----	231μW	----	50μW	4.24mW	0.78W	21μW
FOM	240	20	8.3	----	42.7	76.3	3.84 e.nJ	85	171	110
Supply	0.5V	-----	0.3V	1.1V	1.2V	----	----	----	2.8V	1.8V

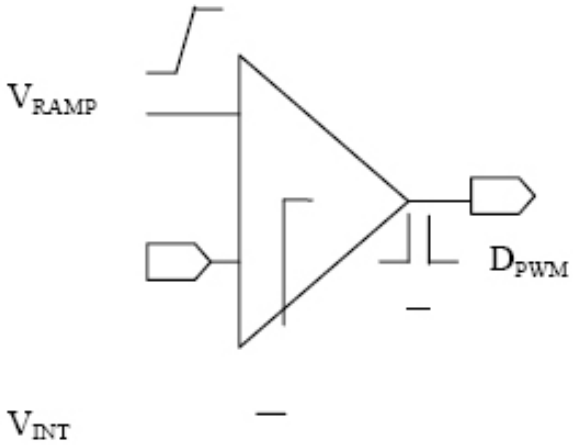


Figure 12. Khatak: Schematic of PWM-ADC.

PMS adopted a less resolution ADC by keeping its operational speed constant just by shifting lower significant bit of the input range by one 1 position in each sample. The delta sigma ADC achieves low noise with multi sampling operation[9] of its modulator and obtains output from low resolution quantizer. Therefore, a PWM delta sigma ADC using a low resolution single slope quantizer is suggested for suppressing the random noise by multisampling operation. Also to reduce the random noise, the programmable gain amplifier is inserted between the pixel array and the given ADC. Figure 12 shows the Schematic of PWM-ADC.

4. Discussion

This section discusses the performance of various above studied architectures depending upon various parameters such as resolution, SNDR, power dissipation etc. In the table number 1 minimum voltage supply for ADC is 0.3V and minimum power consumption is 0.20μW in SAR[3]. FOM is 8.3 and resolution is 8 bit. Energy is directly proportional to the resolution in number of bits. Effective Number Of Bit (ENOB) is another important factor and it can be calculated after calculation of SNDR. ENOB is inversely proportional to the supply voltage. There is one thing to be done in every schematic to optimize the speed and to lower the supply. The result in the Table 1 shows that SAR ADC is ultra low power ADC.

5. Conclusion

ADCs and DACs both play a vital role in digital system therefore; with the progress of digital systems the expectations on the performance of ADCs have been continuously increasing. We have discussed many techniques to improve their performance. The studies so far, show that there is a great possibility to further improve the efficiency of ADCs. This can be done in many ways, such as by reducing their power consumption or, by increasing their conversion speed. Another parameter which affects the performance of ADCs is their area so, we can also improve performance of ADCs by making them area efficient, and various techniques are discussed in brief to do so. Though, some concepts are more theoretical than being practical, because of many complications in their implementation.

To confront these complication more precise techniques need to be explore so that we can optimized scaling, resolution and speed to get a low power high speed precision ADCs.

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