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Design and Implementation of FPGA Based Digital Base Band Processor for RFID Reader

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Abstract

RFID ipso facto deals with identification of objects through radio waves. Its use started during World War II in the identification of "Friend-or-Foe" for targets used by the military, such as aircraft and forces. It was only in 1990s, that large scale use of RFID started. The objective of this paper is to implement the digital baseband processor for UHF RFID reader compatible with EPC Global C1G2 /ISO 18000-6 C protocol. The functional simulation of digital base band processor is done using Modelsim simulator. It is verified and tested successfully on FPGA Spartan-6 prototype board for its logic function. A new bit stream encoding and decoding module are presented for the digital base band processor. The synthesis results proved, that the power consumption of the digital base band processor is about 5mW and the number of slice registers and LUTs used are 32 and 33 respectively. The results presented in this paper are better than literature reported in terms of power. Areas of use RFID were supply management, for tracking articles, inventory and also for identification of animals.

Keywords: CRC, FPGA, HDL, ISO18000-6, RFID, UHF Reader

1. Introduction

Radio Frequency Identification (RFID) is an automatic identification technology that identifies objects automatically using the radio frequency signals. RFID has received much attention as it has rapidly growing with applications such as, animal tracking, toll collection, the building access control, access control, inventory management etc. An RFID ubiquitous application evokes challenges, such as the security and privacy concerns, low power and small size. Several reader digital baseband designs have been presented namely the RFID reader implemented in[1] has good performance, but consumes large power of say 105.215mw. In[2] designed and simulated the reader digital base band processor which consists of transmitter and receiver compatible with ISO 18000-6b protocol. FPGA based digital base band processor is simulated using Verilog code and implemented in[5] which is an identification range of 8~9m with a speed of 110~120 tags per second. In[8] implemented a digital base band processor with a power consumption of 108.45mw. In such systems, the readers provide power to the passive tags by sending continuous signals and interchange message with tags by the propagation of radio frequency signals.

Figure 1 show the general block of the reader system which is divided into RF, baseband and MAC layer sections. The RF section consists of UHF transmitter and receiver, which converts baseband signal into radio frequency signals and inverse. The digital baseband is the brain of the reader and upper level of the Physical Layer (PHY).The digital baseband perform symbol-bit conversion, CRC checking, encoding and decoding. The RF and baseband sections form the PHY layer. The Media Access Control (MAC) layer is operated by the MAC processor which provides interface to the host PC. The antenna is used for receiving and transmitting signal through the air interface.

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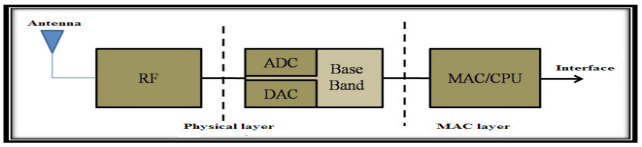

Figure 1. General block of the reader system[3].

In this paper, we present a complete design of UHF reader digital baseband processor. The encoding and decoding mode adopted are bit stream encoding and bit stream decoding. The design can achieve tags identification and adjust received and transmitted data signals perfectly, so that encoding and decoding results are more accurate.

This paper is organized as follows: Section II defines the Architecture of the proposed design. Section III explains CRC method. Section IV describes encoding, decoding methods and power optimization technique. Section V describes Simulation and synthesis results. Finally, conclusion is presented in Section VI.

2. Architecture of the Proposed Design

The proposed architecture of the UHF RFID reader digital baseband system is shown in the Figure 2. The Digital baseband processor of the reader consists of a transmitter, receiver and a controller block. The transmitter of the Digital baseband processor comprises of CRC check module, encoding module, channel filters and the encoded data is up converted and sent to RFID passive tag through the antenna. Receiver module consists of tag response module and decoding module. The data sent by the tag is extracted by the antenna and it is down converted and applied to the receiver there it is processed and sent to the user for taking appropriate action. Control module is responsible for generating control signals for base band processor according to instruction from the user. Each sub modules are explained in the following sections.

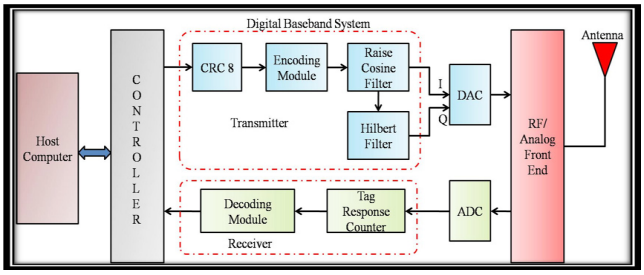

Figure 2. Block diagram of the proposed UHF RFID reader digital baseband system.

3. CRC Method

CRC module is designed to ensure the validity of the data during the data communication. CRC are so called because the value is a redundancy and algorithm is based on the cyclic codes. CRC are popular because they are simple to implement in binary using hardware, particularly good at detecting common errors caused by noise in transmission channel. Cyclic codes are not only simple to implement but have the benefit being particularly well suited for the detection of burst error, contiguous sequence of erroneous data symbol in messages. Polynomial $z^5 + z^3 + 1$ are used to generate CRC5.When the reader sending out data to tags, CRC8 is adopted. Specification of CRC code requires definition of a generator polynomial.

This polynomial becomes the divisor in polynomial long division, which takes the messages as the dividend, and in which the quotient is ignored and the remainder is the result. To compute binary CRC, the input is represented by row of bits, and position the (n+1) bit stream representing the CRC's divisor called a polynomial.

Consider 14 bits of message is to be encoded with 3 bits of CRC, with a polynomial z^3+z+1.the polynomial is written in binary as the coefficient a 3rd order polynomial has 4 coefficients ($1z^3+0z^2+1z+1$).In this case the polynomial coefficient values are 1,0,1and 1.

The message to be encoded: 1101001110110

First padded with zeros corresponding to the bit length highest order of the CRC. Calculation for computing CRC:

1 1 0 1 0 0 1 1 1 0 1 1 0 0 000 ← input right padded by 3 bits

1 0 1 1 ← divisor 4 bits

0 1 1 0 0 0 1 1 1 0 1 1 0 0 000 ← result

The algorithm acts on the bits directly above the divisor in each step. The result for the iteration is obtained by performing bitwise XOR on 4-bits polynomial divisor and the starting 4-bits MSB of the input bits above it. The remaining bits are simply copied directly below. The divisor is then shifted one bit to the right and the procedure is repeated until the divisor reaches the right-hand end of the input row. The entire encoding procedure is shown below:

11010011101100 000 ← input right padded by 3 bits

1011 ← divisor

```
01100011101100 000  <-- result
    1011
    00111011101100 000
      1011
    00010111101100 000
       1011
    00000001101100 000
          1011
    00000000110100 000
           1011
    00000000011000 000
            1011
    00000000001110 000
             1011
    00000000000101 000
              101 1
    000000000000000 100  <-- remainder (3 bits).
```

Division algorithm stops when dividend is becomes equal to zero. The validity of received message can be verified by performing the above calculation again and with the check value is added instead of zeros. The remainder should be equal to zero if there are no errors. In our work CRC8 is design at the RTL level.

4. Encoding, Decoding and Power Optimization Method

The encoding module comprises of an address generator, asynchronous dual port RAM, an encoder counter and a bit stream encoder which is shown in Figure 3. It is utilized to encode data transmitted from the reader to tag. Bit stream encoding mode is adopted in encoding module.

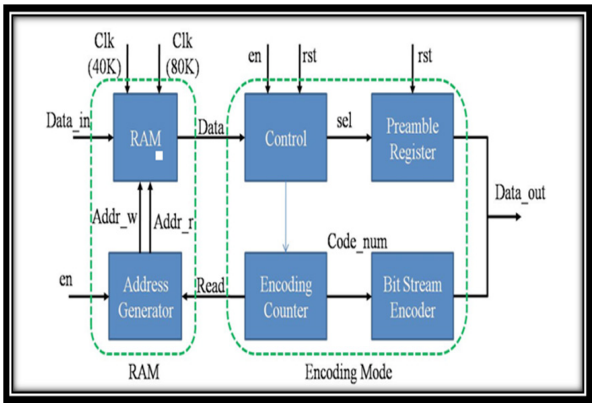

Figure 3. Encoding module of the base band processor.

4.1 Proposed Bit Stream Encoder

Encoding logic is designed to minimize power dissipation by reducing the number of transitions occurring during transmission. In order to achieve this, proposed logic performs operations depending on odd invert condition. The condition is to decide whether the odd inversion has to be applied or not is given by (1). Consider the encoder circuit diagram shown in Figure 4(a), the encoding logic denoted by *'E'* is integrated into the base band processor, which has the deciding authority whether to perform inversion or not. The decision is taken by comparing the previously encoded flit with the flit that is currently being transmitted.

$$T_y > (w\text{-}1)/2 \quad (1)$$

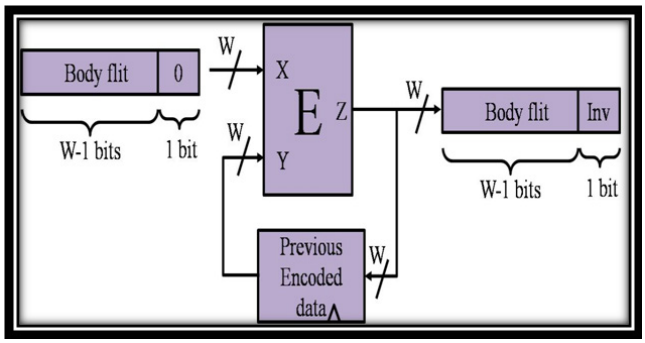

Figure 4 (a). Encoder circuit diagram[12].

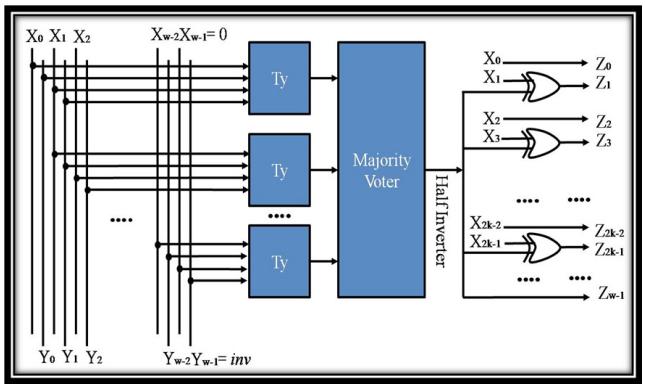

Figure 4 (b). Inside view of the encoder block (E).

Considering generally a data width of w bits, where out of w bits one bit is reserved as inversion bit which helps in indicating whether the flit passing through the encoder is inverted or not. The block *E* has two inputs denoted by X and Y and the output as Z. The current flit to be transmitted is given to the first input X, where the incoming w bits are packed into (*w*-1) bits body flit and a "0" bit (inversion bit). And the previously encoded flit

is given to the second input Y, where the w^{th} bit denoted by inv is used to identify whether it was inverted or not. The inv field is set to "1" when the previous flit is inverted and set to "0" if inversion is not performed. The incoming (previous encoded) body flits of (w-1) bits are represented by X_i (Y_i) where i= 0, 1,2,……., *w*-2. Within the encoding logic two adjacent bits of the input flits are given as the input to the sub-blocks T_y (e.g., $X_0X_1Y_0Y_1$, $X_1X_2Y_1Y_2$,…… ….,$X_{w-2}X_{w-1}Y_{w-2}Y_{w-1}$ where X_{w-1}=0 & Y_{w-1}=inv), when any type of the T_y transition is detected the output is set to "1".Such application of odd inversion over this pair of bits results in the minimization of the power dissipation. The next stage in the encoder is a majority voter block which checks for the condition given by (1) if this is satisfied inversion is performed on odd bits such as X_1, X_3, X_5 so on at the final stage. At the decoder side it simply checks the inversion bit if inv bit is set to "1", it just inverts the received flit.

4.1.1 Encoding Method

The output mainly depends on the previous bit of the input as shown in the above block diagram. Consider the 8-bit input sequence is X=1 0 0 1 1 0 0 1 and X is XOR with half inverter to get encoded output i.e. Z = 0 0 1 1 0 0 1 1

4.1.2 Power Reduction Method

When a data is sent over base band processor is stored in an SRAM cell. Dynamic power is consumed as a result of a capacitive load being charged while transistors are switching.

The dynamic power (P) = $\alpha \cdot C \cdot V^2 \cdot f$ ---------- (2). In equation (2), C is the switched capacitance, P is the power consumed, V is the supplied voltage and α represents the activity. Factor f is the clock frequency that the capacitive load C is charged in a given cycle. In order to reduce the dynamic power, in our work a new method of reducing the activity is adopted which is explained as below.

Present bit can be taken randomly, X=1 0 0 1 1 0 0 1

X= 01 00 10 11 01 00 10 11

Previous bit Y= 00 01 00 10 11 01 00 10

Ty= 1 1 1 1 1 1 1 1

Ty $\geq$ (w-1)/2

8 $\geq$ (8-1)/2 =3.5

The flit can be taken either 3 or 4.

In the encoding method 1 to 0 or 0 to 1 transition can be considered

Consider Half invert = 1

Therefore the number of transition will be three or four instead of eight. Hence the activity factor α is reduced there by dynamic power is also reduced.

4.2 Decoder Module

Decoding module comprises of the tag response unit and decoder unit, whose structure is shown in Figure 5. The decoding mode which is used here is a bit stream decoder. It is utilized to decode the backscattered data from tags to readers.

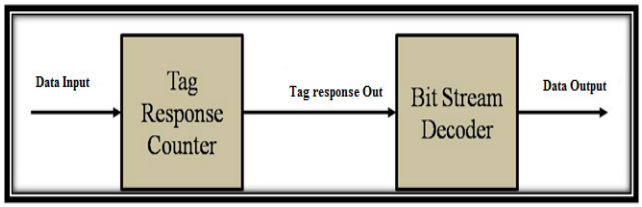

Figure 5. Decoder module.

Consider the encoded output as the input to the decoder as shown below:

Decoder input: Z = 0 0 1 1 0 0 1 1

4.2.1 Power Reduction in Decoder

In order to reduce power, the number of transitions is reduced as follows:

Present bit can be taken randomly as shown below

X= 11 01 00 10 11 01 00 10

Previous bit Y= 00 11 01 00 10 11 01 00

Ty= 0 1 1 1 1 1 1 1

Ty $\geq$ (w-1)/2

7 $\geq$ (7-1)/2 =3

The flit can be taken as 3. Hence now transitions will be just three instead of eight and therefore power will be less.

In the decoding method 1 to 1 or 0 to 1 transition can be considered

Consider Half invert = 1

4.2.2 Decoding Method

The output mainly depends on the previous bit of the input as shown in the above block diagram. Consider the

8-bit encoder output sequence is Z = 0 0 1 1 0 0 1 1 and this Z is XOR with half inverter to get back original data i.e. X= 1 0 0 1 1 0 0 1

Hence it satisfies the encoder input = decoder output

4.3 Filter Module

In our proposed design two filters are used in the UHF RFID reader digital baseband system. They are the raised cosine filter and the Hilbert filter in transmitter block. The raised cosine filter is used to make pulse shape according to specification. The Hilbert filter is adopted to generate I/Q two channel signals.

5. Results and Discussion

The proposed design has been simulated using model sim simulator and implemented on FPGA spartnan-6. For synthesis, we used the EDA tool Xilinx and all sub module simulation results and top module results are shown in the following sections.

5.1 Simulation Result of RAM

When clock is high and write enable is high and choose the address location in the memory, where the data to be store. The input is stored into the given address location, which is written into the corresponding memory location. If write enable is equal to low then read operation is performed. The RAM output results are shown Figure 6.

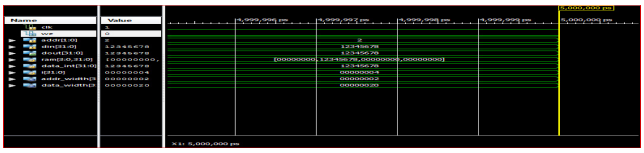

Figure 6. Simulation result of RAM.

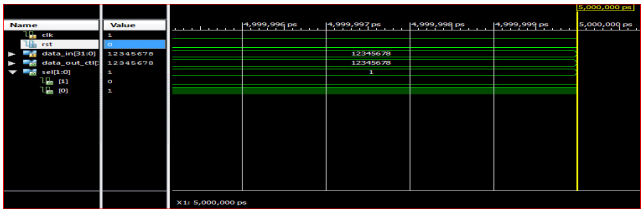

Figure 7. Simulation result of control module.

5.2 Simulation of Control Module

If reset is equal to low, read operation takes place in the RAM, and this output will be applied as the input to the control module. The control module accepts data input and perform selection operation using two select lines. If select line is equal to low, output is given to preamble block. Otherwise this output is applied to the encoder counter. The control module output is shown in Figure 7.

5.3 Simulation of Preamble Register

If reset is equal to one in RAM write operation will be performed therefore no results can be obtained. If reset is equal to zero then it checks for any violation using next count and bit count. The simulation waveform as shown in Figure 8.

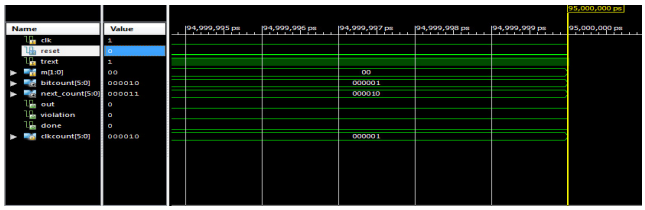

Figure 8. Simulation result of CRC preamble result.

5.4 Simulation of Encoder Counter

Simulation result of encoder counter shown in Figure 9. If reset is equal to one there is no output will be obtained from the encoder counter. Because in RAM only write operation can be done. If reset is equal to 0, then the counter starts counting one by one . The resulting output is given as the input to the bit stream encoder block.

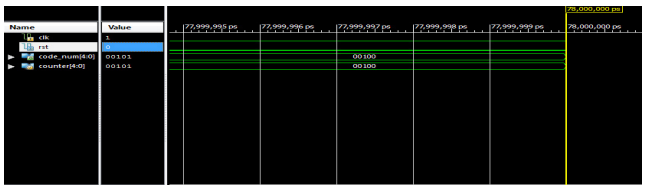

Figure 9. Simulation result of encoder counter.

5.5 Simulation of Raised Cosine Filter

Raised cosine filter is used for removing the unwanted signal occurring from the input data. The input for this filter is 16-bit input data and these are multiplied it with the coefficient to acquire required in-phase result. Hilbert filter can be used for the generation of imaginary signal, which is used for the modulation purpose. The waveforms obtained for raised cosine and Hilbert filters as shown in Figures 10 and Figure 11, respectively.

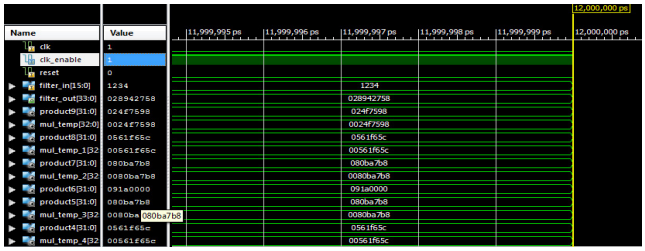

Figure 10. Simulation result of raised cosine filter.

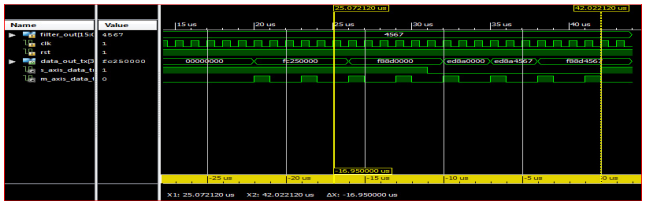

Figure 11. Simulation of Hilbert filters.

5.6 Simulations of Tag Response Counter

Tag response counter is used for removing very high frequency unwanted signal received from the receiver. It takes the input data only from 0 to 255. Because we have taken the input data as 8-bits.The waveforms of tag response counter is shown in Figure 12.

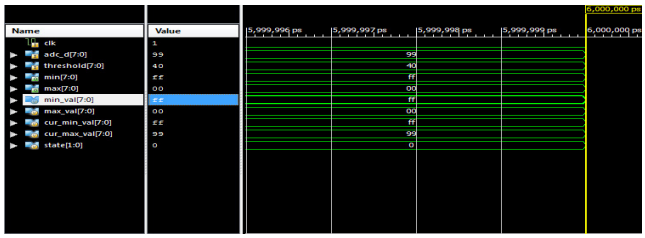

Figure 12. Simulation result of tag response counter.

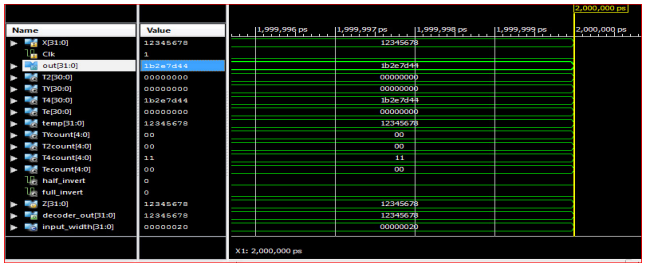

Figure 13. Simulation result of encoder and decoder block.

5.7 Simulation of Encoder and Decoder Block

If reset is equal to 0 whatever the input is given, that will be encoded. This encoder output is applied to the decoder which will be decoded to get the original data. The simulation results of the encoder and decoder block as shown Figure 13.

5.8 Simulation of Complete Design

In the top module. Where the input data applied and is processed in all the modules and the final simulation output and device utilization summary are shown in Figure 14. and Table 1.

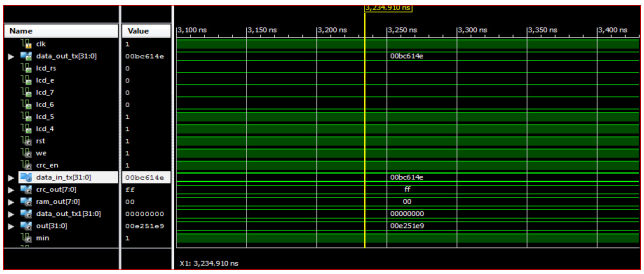

Figure 14. Simulation result of complete design.

Table 1. Device utilization summary of top module

Logic utilization	Used	Available	Utilization
Number of slice register	32	54576	0%
Number of slice LUTs	33	27288	1%
Number of fully used LUT-FF pairs	32	33	96%
Number of bonded IOBS	68	218	31%
Number of BUFG/ BUFGCTRLs	1	16	6%

5.9 Hardware Implementation Result

The complete design of base band processor is tested and verified on FPGA Spartan -6 as shown in Figure 15.

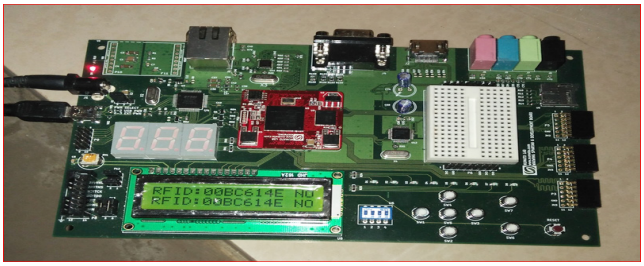

Figure 15. Display hardware implementation results on prototype FPGA device.

Table 2. Performance comparison of the design

Ref.Nos	Dynamic power	Error detection	Coding method	Area	Current	Technology	Decoding method
[4]	6.7mW	CRC5/16	PIE/FM0	NA	5.58mA	ASIC design	Miller subcarrier
[6]	540mW	CRC5/16	PIE/FM0	6mm×6mm	NA	0.18-µCMOS	Miller subcarrier
[7]	8.67mW	CRC5/16	PIE/FM0	18.3mm^2	NA	0.18 µm CMOS	Miller subcarrier
[8]	108.9mW	CRC5/16	PIE/FM0	16.8mm^2	NA	0.18µmSiGeBiCMOS	Miller subcarrier
[9]	105.215mW	CRC5/16	PIE	NA	330mA	0.18 µm CMOS	Miller subcarrier
[10]	1.2 W	CRC5/16	-	21mm^2	NA	0.18µmSiGeBiCMOS	
[11]	276.4mW	CRC5/16	PIE	18.3mm^2	NA	0.18µm CMOS	Bit decoding
Proposed Work	5mW	CRC8	Bit stream	NA	4mA	FPGA design	Bit stream decoding

5.10 Performance Comparison

The performance of the design is shown in Table 2. Compared with other publications it indicates that even though we have used the FPGA design, still power consumption will be better than other publications.

6. Conclusion

This paper presents a UHF RFlD reader digital baseband processor, which includes baseband transmitter and receiver. We proposed an encoding algorithm such as bit stream encoding and decoding methods, in order to optimize power consumption of the digital base band processor. The complete design is simulated, tested and verified on FPGA Spartan-6 board. By comparison with other publications it is shown that our digital base band processor has better performance even under FPGA design. Total number of slice registers and LUTs used are 32 and 33 respectively for the reader digital baseband and the total power consumption is 5mW.

7. Acknowledgement

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