Comparison of Low Power CMOS Voltage Reference Circuit Using Different Types of Charge Pumps

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Abstract

Background: The voltage reference circuits are mainly used in the portable devices like mobiles, laptops for the long battery runtime. Due to this voltage reference circuits the circuit can be operated in the very low supply voltage because of this the power consumption of the circuit can be reduced. **Method Adopted:** In this paper the low power Complementary Metal-Oxide-Semiconductor (CMOS) voltage has been designed by using the conventional charge pump and to achieve the better low power consumption voltage reference circuits and high constant voltage reference different types of charge pumps like Dickson charge pump and the Static Charge Transfer Switch (CTS) charge pump has been replaced in the place of the conventional charge pump. The conventional CMOS volatge reference circuit has the power consumption of 1.007µW and the constant voltage reference of 210mV. **Findings:** By using the Dickson charge pump the power consumption has been reduced to 1.389µW and the constant voltage reference has been icreased to 221mV. Similarly by using by using the Static (CTS) charge pump the power consumption has been reduced to 0.803µW and the constant voltage reference has been icreased to 229.03mV compared to the reference voltage circuit using the conventional charge pump. **Improvements:** The CMOS voltage reference circuit has been designed by using the two types of the charge pump Dickson charge pump and the Static CTS charge pump and all the power consumption and the constant voltage reference circuits has been compared.

Keywords: Charge Pump, Constant Voltage Reference (V_{ref}), Dickson Charge Pump, Static (CTS) Charge Pump, Power Consumption

1. Introduction

The voltage reference circuit is a simple device having the one simple functionality that is it generates the exact output voltage without depending on the factors like input supply voltage, load current, and the temperature change. The voltage reference provides the recommended output voltage which is needed by the circuit for its required measurements¹. The main applications of the voltage reference circuits are used in the Analog to digital converters, servo systems, smart sensors and the portable devices battery systems for the long runtime of the battery. The main block of the voltage reference circuit is the charge pump¹.

Charge pump is an electronic device that changes the input supply voltage V_{dd} to the D.C output voltage V_{out} . It is basically a D.C to D.C converter. The charge pump takes the input as the power supply which is V_{dd} and gives the output as V_{out} which is much superior than the input supply voltage V_{dd}^2 . The output voltage of the charge pump is always higher than the input supply voltage. In traditional D.C to D.C converters uses the inductors where as the charge pump circuit consists of capacitors, switches and diodes which and fabricated on the silicon wafer. The charge pump is basically used in the smart I.C's and gradually scaling down or reducing the input power supply of the I.C's. the charge pump are also used in the integrated circuits like voltage regulators, operational

amplifiers, LCD drivers, antennas etc to reduce the power supply voltage³.

2. Experimental Work

The CMOS voltage reference circuits mainly consists of the charge pump, control unit, comparator. The main aim of the charge pump is to adjust the gate voltages with respect to the comparator output the comparator output is given as the input to the charge pump circuit⁴.

In this section the CMOS voltage reference circuit has been designed by using three different charge pump circuits they are:

- 1. CMOS Voltage reference circuit using conventional charge pump.
- 2. CMOS Voltage reference circuit using dickson charge pump.
- 3. CMOS Voltage reference circuit using static (CTS) charge pump.

1. CMOS Voltage reference circuit using conventional charge pump: The CMOS voltage reference circuit has been designed by the conventional charge pump as shown in the figure 1.



Figure 1. Schematic of conventional charge pump.

By using this conventional charge pump in the CMOS voltage reference circuit the parameters like power consumption and the Constant voltage reference(V_{ref}) has

been improved and the schematic of the CMOS voltage reference circuit using conventional charge pump[9] is shown in the Figure 2:



Figure 2. Schematic of CMOS voltage reference circuit using conventional charge pump.

By using this voltage reference circuit using conventional charge pump the power consumption of 1.007μ W and the constant voltage reference of 210mV. The final output of the CMOS voltage reference circuit using conventional charge pump is shown in the Figure 3.



Figure 3. Output waveform of the CMOS voltage reference circuit.

2. *CMOS Voltage reference circuit using Dickson charge pump:* The CMOS voltage reference circuit has been designed by the Dickson charge pump. The schematic of the Dickson charge pump is shown in the Figure 4.



Figure 4. Schematic of Dickson charge pump.

By using this Dickson charge pump in the CMOS voltage reference circuit the parameters like power consumption has been slightly increased and the Constant voltage reference(V_{ref}) has been improved compared to the CMOS voltage reference circuit using conventional charge pump¹⁰. The schematic of the CMOS voltage reference circuit using Dickson charge pump is shown in the Figure 5:



Figure 5. Schematic of CMOS voltage reference circuit using Dickson charge pump.

By using this voltage reference circuit using dickson charge pump the power consumption of 1.389μ W and the constant voltage reference of 231mV. The final output of the CMOS voltage reference circuit using dickson charge pump is shown in the Figure 6.



Figure 6. Output waveform of the CMOS voltage reference circuit using Dickson charge pump.

3. CMOS Voltage reference circuit using Static CTS charge pump: The CMOS voltage reference circuit has been designed by the Static CTS charge pump. This static CTS charge pump consists of the switches which is useful to increase the voltage boosting. This charge pump can operate at very low input supply voltage¹¹. This Static CTS charge pump is made up of the NMOS switches with ON/OFF characteristics The Static CTS charge pump which is made up of the MOS switches and can operate at very low input supply voltage. The power consumption of the voltage reference circuit using Static CTS charge pump is very less compared to all the designed voltage reference circuits¹².

The schematic of the Static CTS charge pump is shown in the Figure 7.



Figure 7. Schematic of the Static (CTS) charge pump.

By using the Static CTS charge pump the power consumption is very less compared to all the designed voltage reference circuits. The power consumption of this voltage reference circuit using Static CTS charge pump is 803.1nW.The schematic of the voltage reference circuit using Static CTS charge pump is shown in Figure 8.





By using this voltage reference circuit using Static CTS charge pump the power consumption of 0.803μ W which

is very less compared to all the three designs and the constant voltage reference of 229.3mV. The final output of the CMOS voltage reference circuit using Static CTS charge pump is shown in the Figure 9.



Figure 9. Output waveform of the CMOS voltage reference circuit using Static CTS charge pump.

3. Results and Comparison

In the CMOS voltage reference circuit there are two major parameters such as power consumption and the constant voltage reference (V_{ref}). The power consumption of the voltage reference circuit must be less whereas the constant voltage reference (V_{ref}) should be high.

The comparison of the parameters to all the three types of voltage reference circuits are tabulated in the Table 1.

Table 1. Comparison table of different parameter	s.
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Type of voltage reference circuit	Power Consumption(µW)	$\begin{array}{c} \text{Constant voltage} \\ \text{reference}(\text{V}_{\text{ref}}) \end{array}$
Using conventional charge pump	1.007	210
Using Dickson charge pump	1.389	231
Using Static CTS charge pump	0.803	229.3

From the above table the power consumption is very much less i.e 0.803μ W in the CMOS voltage reference circuit using Static CTS charge pump compared to the other two remainig voltage reference circuits and the constant voltage reference (V_{ref}) is high i.e231mV in the CMOS voltage reference circuit using Dickson charge pump.

4. Conclusion

The design of the three different CMOS voltage reference circuits has been designed using three different charges pumps. The proposed design of the voltage reference using CMOS technology with the combination of the comparator, conventional charge pump, and the control unit by using the bulk driven technique and by making all the transistors to work in the sub-threshold region has been designed successfully with the constant reference voltage V_{ref} of 210 mV and with the power consumption of 1.007uW. The same design of the CMOS voltage reference circuit by changing the Charge pump with the Dickson charge pump the constant reference voltage V_{ref} of 231 mV and with the power consumption of 1.389uW and further decreasing of the power consumption the charge pump has been replaced by Static CTS charge pump giving the constant reference voltage $V_{\rm ref}$ of 229.3 mV and with the power consumption of 0.803uW which is very much less than all the voltage reference circuits designed.

5. References

- Byung-Do Yang. 250-mV Supply Subthreshold CMOS Voltage Reference Using a Low-Voltage Comparator and a Charge-Pump Circuit, Proceedings IEEE Transactions on Circuits and Systems—II. 2014; 61(11).
- Malcovati P, Maloberti F, Fiocchi C, Pruzzi M. Curvature Compensated BiCMOS Bandgap with 1-V Supply Voltage. Proceedings IEEE Journal of Solid-State Circuits, 2001; 36(7):1076–81.
- Ivanov V, Brederlow R, Gerber J. An Ultra Low Power Bandgap Operational at Supply from 0.75 V, Proceedings IEEE Journal of Solid-State Circuits. 2012; 47(7):1515–23.
- Yang Y, Binkley DM, Li L, Gu C, Li C. All-CMOS Subbandgap Reference Circuit Operating at Low Supply

Voltage. Proceedings IEEE International Symposium on Circuits And Systems, 2011; p. 893–896.

- Kinget P, Vezyrtzis C, Chiang E, Hung B, Li TL. Voltage References for Ultra-Low Supply Voltages. Proceedings IEEE Czustom Integrated Circuits Conference. p. 715–20.
- Magnelli L, Crupi F, Corsonello P, Pace C, Iannaccone G. A 2.6 nW, 0.45 V Temperature-Compensated Subthreshold CMOS Voltage Reference. Proceedings IEEE Journal of Solid-State Circuits. 2011; 46(2):465–74.
- Yutao Wang, Zhangming Zhu, Jiaojiao Yao, Yintang Yang. A 0.45-V, 14.6-nW CMOS Subthreshold Voltage Reference With No Resistors and No BJTs. Proceedings IEEE Transactions on Circuits and Systems—II. 2015; 62(7): 621–25.
- Alan Rich. Voltage Reference Application and the Design Note, AN177.0, June 23, 2005.
- Gaetano Palumbo, Domenico Pappalardo. Charge Pump Circuits with only Capacitive Loads: Optimized Design, Proceedings IEEE Transactions on Circuits and Systems— II. 2006; 53(2).
- Hongchin Lin, Nai-Hsien Chen Bellos. New Four-Phase Generation Circuits for Low-Voltage Charge Pumps, Proceedings of the IEEE International Symposium on Circuits and Systems. 2001; 1.
- Ming-Dou Ker; Shih-Lun Chen; Chia-Shen Tsai. Design of Charge Pump Circuit with Consideration of Gate-Oxide Reliability in Low-Voltage CMOS Processes. Proceedings IEEE Journal of Solid State Circuits. ,2006; 41(5).
- Ming-Dou Ker, Shih-Lun Chen. Ultra-High-Voltage Charge Pump Circuit in Low-Voltage Bulk CMOS Processes with Polysilicon. Proceedings IEEE Transactions On Circuits And Systems—II. 2007; 54(1).
- Mostafa H, Ismail Y. Circuit Design Techniques for Increasing the Output Power of Switched Capacitor Charge Pumps. Proceedings IEEE 27th Canadian Conference on Electrical and Computer Engineering (CCECE). 2014; 1–5.
- 14. Mengshu Huang, Leona Okamura, Tsutomu Yoshihara. Charge Sharing Clock Scheme for High Efficiency Double Charge Pump Circuit, Proceedings of 10th IEEE International Conference on Solid State and Integrated Circuit Technology(ICSICT) 2010; p. 248–50,
- Robert C Chang, Lung-Chih KUO, A New Low-Voltage Charge Pump Circuit for PLL. Proceedings IEEE International Symposium on Circuits and Systems. 2000; 701–05.