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Improving breakdown voltage in LDMOS with doped silicon pockets in buried oxide

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Abstract

An SOILDMOS device with a new technique of having doped silicon pockets in SOI buried oxide is presented in this paper. The doped silicon pockets reduce the effective electric field in the top silicon layer by forming a depletion region between the pockets and the drift region, thereby improving the device breakdown voltage and reducing specific resistance. The device simulations are carried out in an open source TCAD software package. The effective values of doping, device geometry is found and the device structure is developed. The modeled device gives a breakdown voltage of 79.5V, specific resistance of 23.4mΩ-mm2 and FOM of 27MW/cm. The device is shown to have a threshold voltage of 4V making it suitable for high voltage technology. Performance comparison with currently available Commercial LDMOS devices is also presented.

Keywords: Breakdown Voltage, Doped Silicon Pockets, Figure of Merit (FOM), RESURF, SOI-LDMOS, Specific Resistance

1. Introduction

LDMOS (Lateral Double-Diffused Metal-Oxide-Semiconductor-Field-Effect-Transistor) is a mature technology with its long usage in the wireless industry and has an excellent reliability record[1]. The main driver for LDMOS is its high volume application, which enables continuous improvement of the LDMOS technology[2,3]. LDMOS is a preferred technology for high power applications when compared with other competing technologies like GaAs and GaN[4] with process compatibility to BCD (Bipolar-CMOS-DMOS) technology as well[5]. The extended drift regions in the LDMOS device enable high voltage with standing capability[6]. The Reduced Surface Field (RESURF) technology also further enhances the device breakdown voltage[7].

Smayling and Torennogavea method to fabricate the LDMOS device[8]. A self aligned RESURFLDMOS was fabricated and demonstrated by Mosher[9]. An LDMOS device for 32V LDMOS technology with a power performance upto 130Win2.7-3.5GHz frequency band with a

36% drain efficiency was demonstrated by Formicon[10]. A SiLDMOS power amplifier with 45% power efficiency was demonstrated in[11].

Use of silicon on insulator (SOI) technology has been investigated by many researchers[12-14] to achieve an

Improvement in the device breakdown voltage. SOI device has a lower vertical breakdown voltage and limited thickness of the active silicon layer posing challenges for the LDMOS design[15-17]. Interface charges at the buried oxide inter face result in a uniform electric field distribution in the horizontal direction[18]. Incorporating accumulation regions in the drift region improves the vertical electric field. However, the buried oxide in the SOI technology blocks the heat transfer from the surface to the substrate causing self heating.

In this paper, a new device structure is proposed with an aim to improve the breakdown voltage and specific

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resistance in a SOI process. As the SOI devices have lower vertical breakdown voltage, it is attempted to alter the doping in the top silicon layer of SOI wafer, so that the effective electric field gets reduced and hence the breakdown voltage improves. The electric field is altered by fabricating pockets of doped silicon in the buried oxide layer at the Si-buried oxide interface. The pockets of doped silicon form a depletion region with the drift region altering the electric field distribution and hence the breakdown voltage.

2. Conventional LDMOS

LDMOS transistors are voltage controlled devices, hence unlike the bipolar devices, there is no gate current flowing the gate. Hence the bias circuitry is very much simplified as compared to the bipolar devices. The majority of the LDMOS devices have the source connected to the backside of the device. Hence, the requirement of toxic BeO (Beryllium Oxide) packages is eliminated. The bulk source can be eutectic ally soldered to the package and the bond wire requirement is removed reducing the inductance. The LDMOS devices show better temperature stability than the bipolar devices. Also they provide device stabilization preventing oscillations at higher frequencies. Across section schematic of the conventional LDMOS is shown in Figure 1.

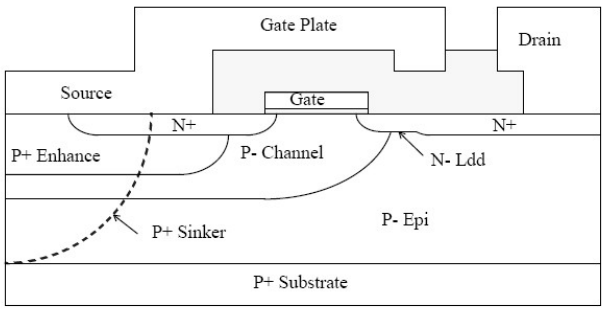

Figure 1. Conventional LDMOS device structure.

The device has a sinker diffusion connecting the source to the back side substrate. The device consists of a drain extension which helps realize higher breakdown voltages. The drain is shielded from the gate by metal field plate realizing extremely low feedback capacitance. The higher breakdown value in LDMOS is due to the RESURF technology. In RESURF, one horizontal p^-n junction and a vertical p^+n junction develop two diode structures. The vertical diode shall have a lower breakdown voltage determined by the epitaxial doping level. The horizontal junction breakdown voltage is higher due to the high ohmic substrate. At thinner layers of the epitaxial layer, the depletion of the vertical junction becomes more and more reinforced by the horizontal junction. Hence for the same applied voltage, the depletion layer stretches along the surface longer than expected from one-dimensional calculation. After a certain thickness, the reduced surface field does not reach the critical value even at high voltages and hence the breakdown is eliminated or raised to very high voltages. This forms the basis of an increased breakdown voltage LDMOS device.

3. Related Work

A brief of the commercially available LDMOS devices is presented in this section.

In[19], ap-implant layer is additionally considered to improve breakdown voltage of 0.18-µm high voltage (HV) RESURF LDMOS, manufactured by Maxchip Electronics Corporation. Inclusion of p-implant layer improved the breakdown voltage and eliminates the additional fabrication step overhead. A 12% increase in breakdown voltage is reported.

National Semiconductor's PVIP25 technology proposed shallow trench isolation (STI) to improve the performance of high voltage LDMOS device[20]. By incorporating STI technique, break down voltage, hot carrier lifetime, safe operating area improvements are reported for both PLDMOS and NLDMOS.

Alow cost solution using a two-step oxideprocess to improve the performance of the conventional 0.18-µm BCD technology based Rich tekNLDMOS device is proposed in[21]. A thin oxide layer (referred to as adjusted oxide layer) with an optimized profile is considered near the channel region. The oxide layer below the channel enables to optimize the specific on resistance. A thick isolation oxide layer is

considered to minimize specific resistance when breakdown voltage increases. The two-step oxide process aids in low power consumption and can be achieved by mere 3 additional mask steps.

In recent years, use of buried oxides to improve the

Breakdown voltage is proposed. The modulated electric field observed at buried oxide enables in achieving high breakdown voltages. The simulation results presented

prove that by using buried oxide pockets, higher device breakdown voltages can be achieved. The proposed device also exhibits low switching delays, hence useful for high frequency applications[22].

In order to improve specific resistance and breakdown voltage of conventional LDMOS devices, a dual protruded silicon dioxide is considered in the drift region. Due to the dual protruded oxide, peaks in the electric field profile are observed that aid in improving the breakdown voltage[23]. In addition to the dual protruded oxide layers at hreep-windows are also considered to improve performance. Simulation results presented exhibit improvement in electric field, specific on-resistance and breakdown voltage when compared to conventional LDMOS structures[24].

Inspired by discussions presented in[22,23] and[24] a novel LDMOS structure is proposed in this paper and is discussed in the following section.

4. Proposed LDMOS Structure

The device schematic of the proposed structure is shown in Figure 2. The LDMOS device basically is fabricated on a SOI substrate. The salient deviation from the standard SOI- LDMOS structure is the presence of doped silicon pockets at the interface of buried oxide and the drift region. For an n- channel LDMOS, p^+ doping is used for the pockets. Multiple p^+ pockets are fabricated in the buried oxide. The length and width of the pockets are kept equal to simplify process and simulation.

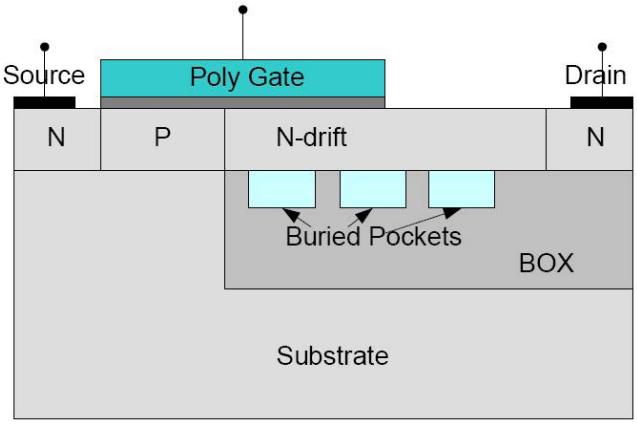

Figure 2. Schematic of proposed LDMOS device.

Process simulations are carried out by solving Poisson's equations and drift/diffusion equations. Shockley-Hall-Read (SHR) and Auger models are used for carrier generation and recombination and impact ionization. The carrier velocity saturation, carrier-carrier scattering in the high doping concentration regions, mobility dependence on temperature and electric field are also considered. The analytical models used for various processes and numerical computation are listed in table 1.

Table 1. Process models for simulation

Process	Model
Diffusion	GAUSSIAN
Implantation	PEARSON
Drift-diffusion solver	GUMMEL,NEWTON
Mobility	LombartiCVT
Carrier generation & recombination	Shockley-ReedHall
Impactionization	Selberrherr(SELB)

PEARSON model is used for ion implantation process as it is most suitable for asymmetrical implantation profiles. This function is used to obtain the longitudinal implantation profiles. The implantation profile as per the Pearson function is given by the differential equation:

$$\frac{df(x)}{dx} = \frac{(x-a)f(x)}{b_0 + b_1 x + b_2 x^2}$$

Table 2. LDMOS device fabrication process steps

Step	Description
0	Starting material initial p-type substrate
1	Partial buries oxide using SIMOX
2	Silicon pockets in buries oxide using SIMOX
3	Boron Implantation in pockets
4	Gate oxide deposition by dry oxidation
5	patterning and Poly silicon gate deposition and patterning Phosphorus diffusion for poly gate and S/D region
6	Contact electrode area patterning and metal deposition

The device process flow is shown in table 2. Starting substrate is a <100> oriented p-type silicon wafer. A partial SiO2 layer is to be created with a separation using SIMOX method. The thickness of SIO2 layer is 1.3μm. In the next step, the p^+ windows are created by SIMOX process. Next boron is added by ion implantation to have p^+ windows. A thermal annealing process reduces inter face traps and improves crystalline silicon for source,

drain and drift regions. The process details are mentioned in table 3.

Table 3. Process parameters

Step	Processparameters
Substrate	Boron doped 1x 10^{14} cm^{-3} <100> orientation
1	Deposit Partial SiO2 (2µm) usinf SIMOX process
2	Grow Pockets in SiO2 using SIMOX process
3	Boron Implant for doped pockets 5 x 10^{18} cm^{-3} Ramp up: Time: 1min, 800^0 C to 1000^0 C Coast: Time: 10 min, 1000^0 C Ramp down: Time: 1min, 10000 C to 800^0 C
4	Gate oxide 0.05 µm Poly: 0.2µm, Doping: Phosphorus, 1x 10^{20} cm^{-3}
5	S/D Phosphorus Implant: Dose 1x10^{19} cm^{-3}, Energy: 25ke V Thermal Anneal: Time: 1min, 950^0 C
6	Deposit Aluminum metal for contacts

5. Simulation & Results

The simulated device geometry is shown in Figure 3. Three pockets of doped silicon are fabricated in the buried oxide layer below then-drift region. The region of interest is the top silicon layer and the buried oxide layer below then-drift region. The dimensions of the pockets and their spacing are kept equal. Fine meshing is used in the areas near the junctions while coarse meshing is used in other regions. This helps reduce the computational loads till maintaining the required details at critical areas. Meshed structure is shown in Figure 4.

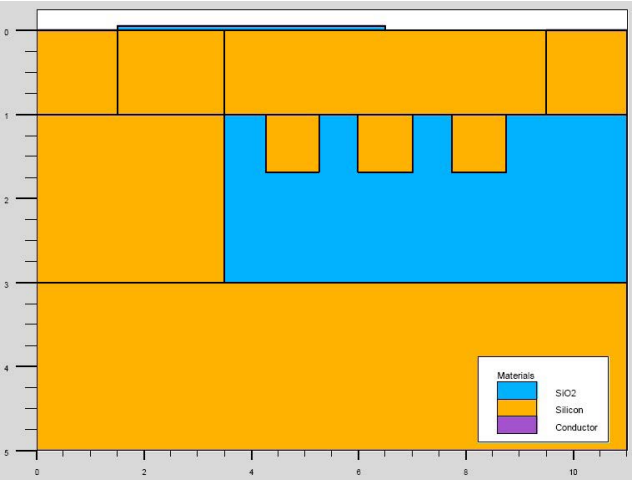

Figure 3. LDMOS device structure from process simulation

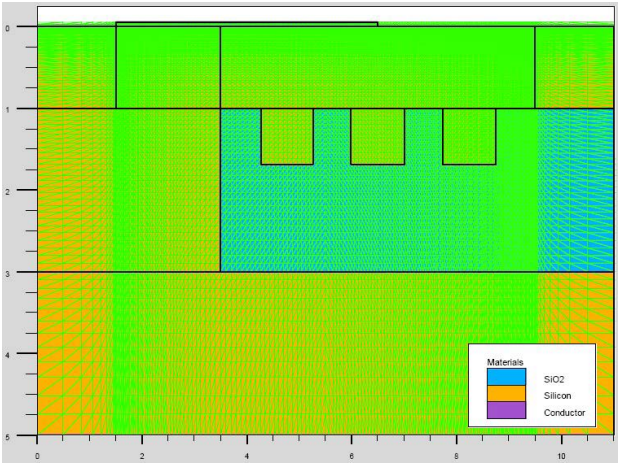

Figure 4. Meshing for device simulation.

Doping profiles for the LDMOS device structure are shown in Figure 5 complying with the values in Table III. Three pockets of doped silicon in buried oxide can be observed as proposed in the process flow. The device structure is simulated for the performance characteristics.

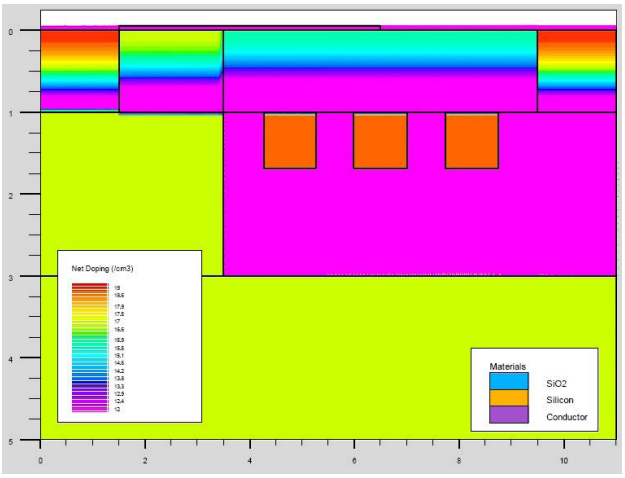

Figure 5. Net doping in proposed LDMOS device.

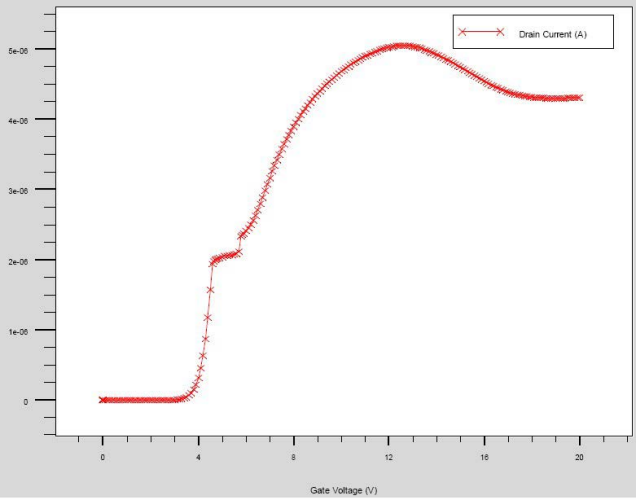

Figure 6. Simulated Id-Vgs plot for LDMOS.

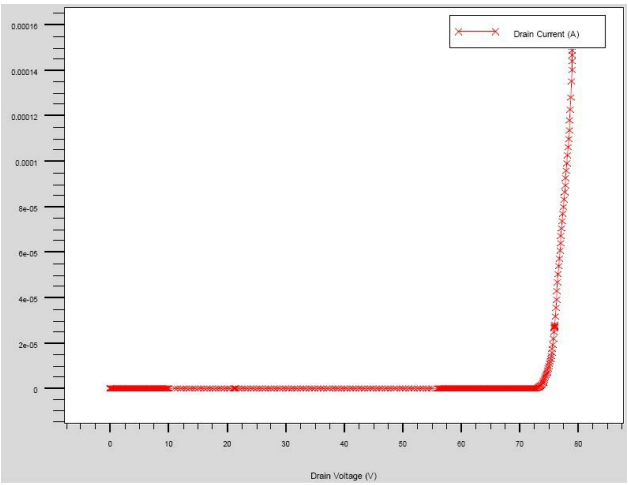

Figure 7. Simulated breakdown in LDMOS device.

Stays in cut-off region for gate voltages below 4V. The drain current saturates at higher gate voltages.

Another important feature of the LDMOS device is the breakdown voltage. The device breakdown is simulated by applying a drain voltage to the device, keeping the gate open (OFF). The drain voltage is increased in steps and the drain current recorded. The results are shown in Figure 7. The drain current is almost constant at low values for drain voltage. As the drain voltage is increased beyond 70V, the drain current increases abruptly to high values. At drain voltage of around 79.5V, the device drain current increase suggests avalanche breakdown.

Figure 8 shows the electric potential distribution in the device under breakdown condition. The maximum potential drop occurs at the edge of then-drift region. This suggests that the electric field is higher in this region. Electric potentials are of low values in the other regions in then-drift region. The potential distribution shown in Figure 7 is suggestive of device breaking down at the drain edge of the drift region.

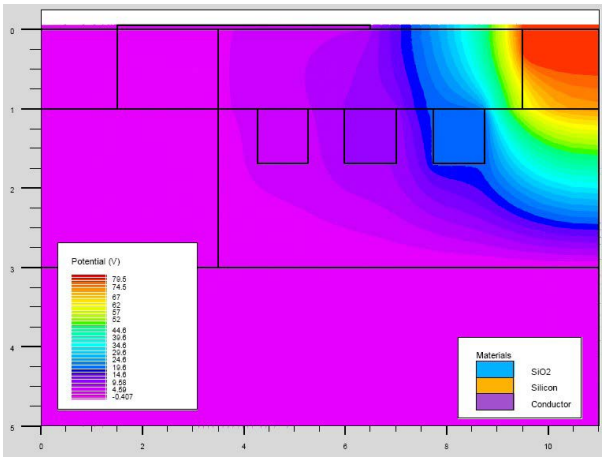

Figure 8. Electric Potential distribution under breakdown condition.

Figure 9 shows the electric field distribution in the device under breakdown conditions. The higher values of electric field are observed in the drain end of n-drift region. The critical electrical field values for silicon are reached near the drain junction. The electric field in other places is very low. The p^+ pockets in the buried oxide effectively enhance the electric field in the insulating buried oxide layer and reduce the field in the active silicon layer. This lowers the electric field in this region and thereby increases the breakdown voltage. The doped silicon pockets extend the depletion region in the n-drift area of the device and modify the electric field distribution, thereby increasing the breakdown voltage.

The Id-Vgs plot is shown in Figure 6. The simulated characteristics plot shows threshold voltage of 4V. The device the electric field distribution is lower and more uniform in the active silicon layer with smaller peaks demonstrating the effect of doped pockets. The extension of depletion region in the drift region results in more uniform electric field.

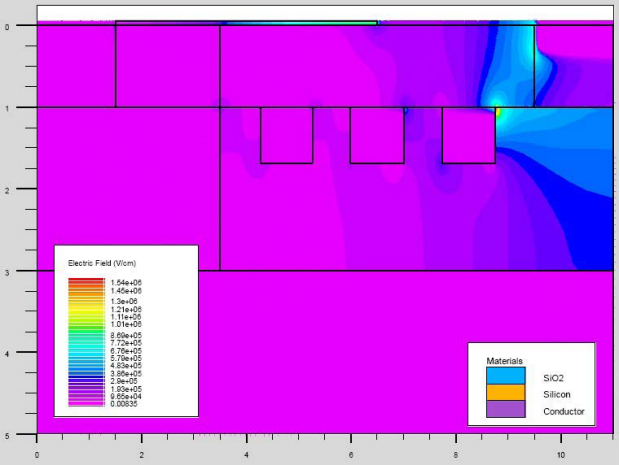

Figure 9. Electric field distribution in LDMOS device under breakdown

Another affect of doped silicon pockets is on the specific resistance of the device. The extension of depletion region into the n-drift region results in lowering of the on resistance, a required characteristic. The reduction in on-resistance is normally associated with degradation in breakdown voltage. However, in this case the breakdown voltage has improved. The doped silicon pockets act as source of ionized carriers to the depleted drift region, thus maintaining the charge balance in the depleted drift region.

The current density value for the proposed device is 4.27×104A/cm2. The specific resistance is the sum of the resistance of the source, channel drift region and drain of the device. The specific resistance of the device is calculated to be 23.4mΩ-mm2. The FOM for the proposed device is 27MW/cm^2 calculated as the ratio of breakdown voltage to square of specific resistance. The doped pockets help reduce the specific resistance without reducing the breakdown voltage.

5. Comparison Notes

Breakdown Voltage and the effective resistance of the device are considered for the comparison of the proposed device with other works as described in[20-25].

The performance comparison is compiled and presented in table 4. The best performance is given in[21] which is 15% lesser than the proposed LDMOS device. A performance enhancement of 48% is achieved as compared to our previously reported design[25,27]. Higher breakdown voltages and comparable on-resistance are achieved as compared to[19]. Authors in[21] have reported 36VDMOS and 45VDMOS structures exhibiting best in class R on performance when compared to commercially available conventional LDMOS devices offered by various fabrication houses. The proposed LDMOS has a 66% higher breakdown voltage when compared to 36VDMOS[21] with comparable specific resistance.

Table 4. Performance comparisons considering breakdown voltage and specific resistance

Device Name	Break down voltage	On Resistance
Conventional HV LD-MOS, Han[19]	25.8V	13.3m Ω × mm^2
LDMOS (0.48 μm × 3.0μm), Han[19]	28.9V	14.2mΩ × mm^2
POR, Haynie[20]	29V	300Ω
New Etch + ISSG, Haynie[20]	29V	277Ω
45VDMOS, Huang21	68V	33.7mΩ×mm^2
Chip film LDMOS, Sunitha[26]	46V	--
SOILDMOS. Bawedin[26]	29V	--
Sunithaet.al.[27]	54V	29.2mΩ×mm
Proposed LDMOS	79.5V	23.4mΩ × mm^2

7. Conclusion

The present work is continuation of the work on LDMOS devices with higher breakdown voltages for flexible electronics kind of applications. The innovative method to insert pockets of doped silicon in SOI-buried oxide layer at the Si-buried oxide inter face has reported improvement in breakdown voltage and specific resistance at the same time. The enhancement of breakdown voltage is attributed to the more uniform distribution of electric field in the n-drift region. The enhancement in specific resistance is attributed to the formation of depletion region in the n-drift region and the doped pockets acting as sources of charge carriers for charge balance.

The process steps to realize the proposed device starting with a SOI wafer obtained using SIMOX process is presented. The fabrication process is simulated in TCAD and the device structure as proposed is obtained. The model is simulated for the device performance and different device characteristics are reported. An improvement in two salient characteristics of LDMOS device: breakdown voltage and specific resistance are reported. The proposed device has a threshold voltage

of 4V and the reports a breakdown voltage of 79.5V. The device specific resistance is 23.4mΩ-mm2 and FOM of 27MW/cm2. A comparison with other reported literature shows significant Improvements in both the characteristics. Moreover, the improvement in specific resistance is achieved without affecting the breakdown voltage of the device.

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