Indian Journal of Science and Technology, Vol 8(23), DOI: 10.17485/ijst/2015/v8i23/71855, September 2015
ISSN (Print) : 0974-6846
ISSN (Online) : 0974-5645

Improved Efficiency 2.4 GHz Class-E Power Amplifier with Improved Controlled Output Power

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Abstract

Background/Objective: High efficiency power amplifiers must provide the required power for signal transmission. Class-E PA is a nonlinear switching type PA which can ideally achieve 100% efficiency. High efficiency and low level output power design of power amplifier is a requirement for optimization of the energy efficiency of the transmitter. **Methods/ Statistical Analysis:** Modified class-E structure with low output power is presented in this paper which is able to deliver low output power with high efficiency. This structure uses a π matching network. **Findings:** Some advantages of proposed power amplifier are the possibility of on-chip implementation, proper power efficiency, improved controlled output power and application in short-range wireless sensor networks. In the proposed power amplifier, controlled output power line is connected with bias voltage input transistor that efficiency of power amplifier is improved in the overall range. In this paper, a 2.4 GHz class-E power amplifier structure with high efficiency has been designed. Maximum output power of the proposed amplifier is 46 mW with maximum added power efficiency of 49%. **Application/Improvement:** The proposed power amplifier is appropriated in short range wireless sensor networks. It has the capability to control output power from 1.75 to 46 mW with 4 to 49% efficiency. The structure has been designed and simulated using 0.18 um CMOS technology.

Keywords: Class-E, Efficiency, High, Output, Power, Amplifier

1. Introduction

Transceivers for wireless sensor network have lately spurred lots of researches and developments. Energy consumption of transceiver block of wireless sensor network must be as low as possible like all other block of the system[1-3]. One of the important challenges of design wireless sensor network transceivers is design of high efficiency power amplifier section. Considering these points, power amplifier is one of the most important blocks of the transmitter which contributes the most power consumption of the transmitter. Proper power Added Efficiency (PAE) of the power amplifier, finally, leads to optimum efficiency of the transmitter structure.

Among power amplifier topologies, class-E power amplifier ideally has 100% efficiency. It has been analyzed in[3-10]. In most of the reported power amplifiers, the challenge was to optimize power efficiency of amplifiers at high output power about 23 dBm to 33 dBm[11-16]. To optimize the energy efficiency of transmitter in wireless sensor networks, power amplifier with low output power and high efficiency is needed. For short-range networks like ZigBee, the required output power ranges from 0 dBm to 10 dBm[17-20] and for body wireless sensor networks, it is even less than 0 dBm. Also, because of changing distances between transmitters and receivers in wireless sensor networks, their transmitter must be able to control the output power to decrease transmitted power in short distances and use less energy for data transmission.

Because of its high efficiency, keying structure is popular in design of radio frequency transmitters. It is proper for constant amplitude power transmission like FSK and PSK modulation schemes.

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In transmitters of wireless networks like wireless sensor networks power control lines are used. Different methods exist for output power level control. For example, with changing supply voltage the transmitted power can be controlled. Figure 1 shows different methods for controlling output power. In design of transmitter control lines must be considered for adjusting output power.

In this paper, section 2 contains the analyses of the proposed power amplifier structure. In section 3, a power amplifier working at 2400 MHz and maximum output power of 46 mW has been proposed. This section, also, includes the simulation results. In final section, conclusion is presented.

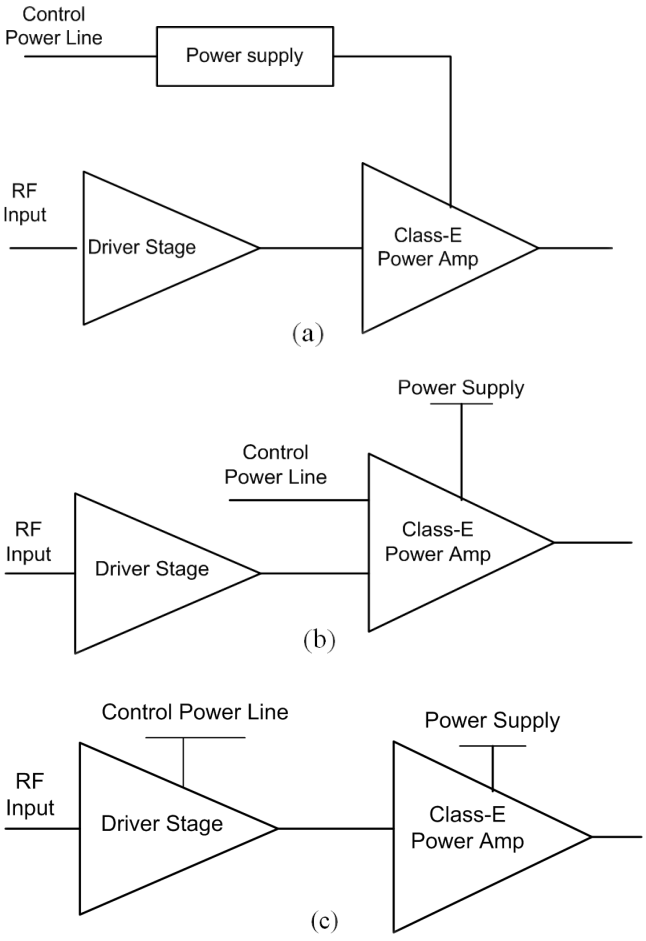

Figure 1. Block diagram of power amplifier a) power supply control b) with control line in output stage and c) with control line in driver stage.

2. Analyses of Power Amplifier Structure

In conventional class-E power amplifier, a big inductor is used to produce constant current. In structure presented in[4] shown in Figure 2a, impedance of the right part is supposed to be Zx. Normally, a series resonance network is employed to omit the harmonics. In our proposed amplifier, the structure of Figure 2b has been used. In this power amplifier, output networks is designed such that for harmonic cancellation Xp (w0)>Xp (nw0) and Xs (w0) <Xs (nw)=0) is needed. In these conditions, cancellation ratio depends on the ratio of Xp (w0) / (xp (nw0)+Xs (nw0)+req) to Xp (w0)/Xp (w0)+Xs (w0)+Req) for n>2. In these conditions network requires a capacitive and an inductive network.

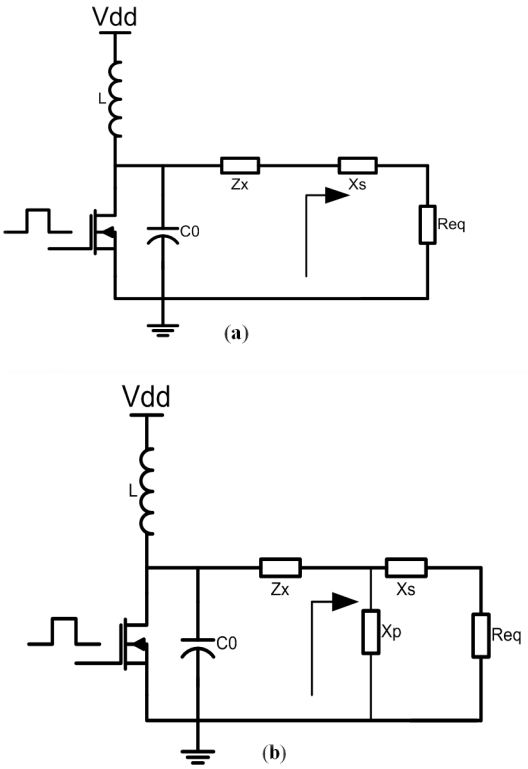

Figure 2. Class-E power amplifier circuitry, a) conventional and b) modified.

Figure 3 shows the proposed power amplifier. Transistor M1 works as on-off switch. In each period, it is switched on and off. The series transistor M2, works like a common gate stage and it is always in on condition. Typically, self-bias cascade structure is used to divide voltage between common gate and common source transistors and solve the limitation of breakdown voltage problem at high output voltages. The existence of transistor M2 provides more isolation between input and output. Capacitor C2 creates a path for harmonic cancellation. Capacitor C3 and inductors L1 and L2 create a matching network for resistor Req at required

frequency w_0. In Figure 3, harmonic cancellation ratio is proportional to Req / (Req+Xs (nw0)) where nw0 is the nth harmonic generated by the amplifier. For better cancellation, we increase Xs or in fact L1.

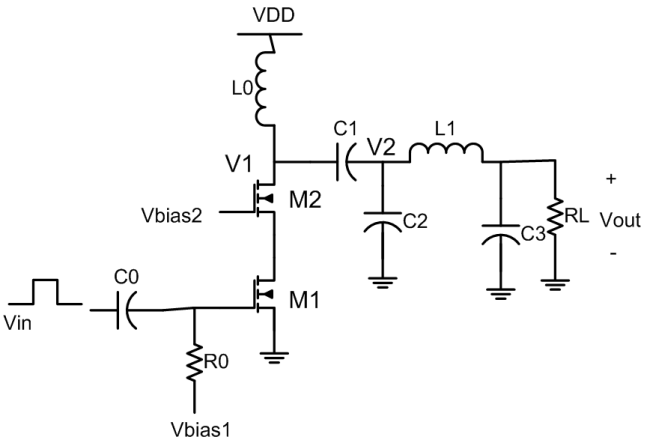

Figure 3. Structure of the proposed power amplifier.

In this amplifier, different methods can be used to adjust the transmitted power. The first one is a circuit that provides the ability to control power supply of the power amplifier. Another method to change the level of output power is using the bias of transistor M2. Actually, in this method the on-resistance of the switch is changed. As a result the current produced in inductor L0 can be decreased or increased which provides the ability to control the output power. Also in this amplifier, output power can be changed by varying the DC value of the input (driver) signal. In this method, the input signal must be sinusoidal because this technique changes the on-time of the transistor M1 or duty cycle of the amplifier. If we suppose that the stimulating signal is sinusoidal and applied to the gate of M1 and incorporate the bias voltage in DC offset of the signal then the input signal can be written as (1):

$$V_g(t) = V_{bias} + V_1 \sin(\omega t) \quad (1)$$

In equation 1, Vth is the threshold voltage of the transistor, w is the angular frequency of the input and V bias is the constant voltage of M1 bias. Considering the Figure 4, M1 is on when the gate-source voltage is equal to threshold voltage. Transistor is on at t1 and is off after t2. So we can write:

$$V_g(t_1) = V_{bias} + V_1 \sin(\omega t_1) = V_{TH} \quad (2)$$

$$DT = t_2 - t_1 = \frac{2}{\omega_{in}} \sin^{-1}\left(\frac{V_{TH} - V_{bias}}{V_1}\right) \quad (3)$$

DT is the duration of on time. T is the period of the input signal. Equation 3 shows that if bias voltage is changed D will be changed, too.

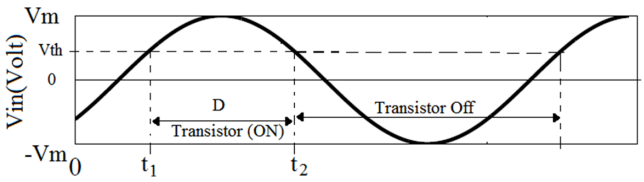

Figure 4. Input signal wave form showing on and off time of the transistor.

Figure 5 depicts the variation of D versus the bias voltage. As reported in[21], equation 4 shows that output power is a function of D.

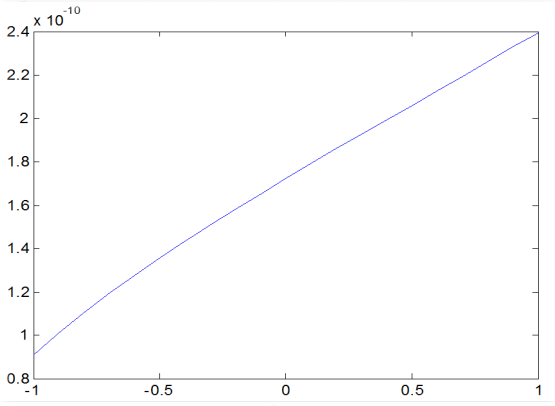

Figure 5. Variations of on-time of the transistor with input signal at 2400 MHz frequency and 2 V amplitude, 0.55 V threshold voltage for bias voltage between -1 to 1 V.

$$P_{out} = \frac{\beta^2}{2\alpha^2}\frac{V_{DD}^2}{R} \quad (4)$$

In this equation, Vdd is power supply voltage and R is the load resistance and α and β are defined as below:

$$\alpha = -\theta_F\theta_c \sin\theta_X + 2\theta_c \sin\frac{\theta_D}{2}\theta_c + (\theta_F \cos\frac{\theta_D}{\theta} + 2\sin\frac{\theta_D}{\theta})\cos\theta_c \quad (5)$$

$$\beta = [\sin\theta_x + \sin(\theta_D - \theta_X)]^2 \quad (6)$$

θd is the time that transistor is on.

$$\theta_D = 2\pi D \quad (7)$$

And θf is the time that transistor is off.

$$\theta_F = 2\pi(1-D) \quad (8)$$

θx is the angular phase difference and defined as below:

$$\theta_X = tan\frac{1-cos\theta_D}{2\pi-\theta_D+sin\theta_D} \quad (9)$$

θc is defined with equation 10.

$$\theta_c = \theta_D / 2\text{-}\theta_X \quad (10)$$

Figure 6 shows the variation of output power versus D.

To compare the ability to control output power a figure of merit must be defined. The best case is that for whole output range PAE is proper and does not change very much. For this purpose, CPO is defined as:

$$CPO = Average\ [P\ A\ E\ (\%)\ ]x\ DR\ [P_{out}(mW)] \quad (11)$$

In equation 11, DR [Pout] is output power variation range and Average [PAE (%)] is the Average Power Efficiency at whole output power range. In fact, this number shows the variations of PAE for variations of output power. The bigger this number the better is the ability to control output power. Furthermore, the PAE curve versus output power can be used to compare different output power control methods.

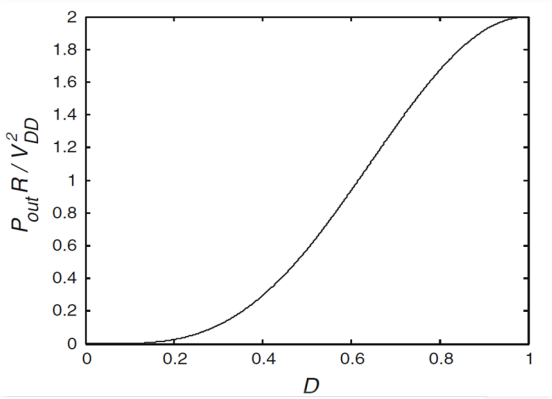

Figure 6. Pout.R/Vdd^2 variations versus duty cycle D[18]

3. Power Amplifier Simulation Results

Power amplifier proposed in this paper has a proper output power for wireless sensor network applications with proper efficiency. All components of this amplifier can be integrated on-chip. The circuitry is shown in Figure 3. According to frequency band of short range wireless sensor networks like Bluetooth and ZigBee, the amplifier has been designed for 2400 MHz. The value of all components is listed in Table 1. Figure 7 shows the waveforms of nodes V1, V2, output voltage and power supply current for one period. Power supply can be controlled to adjust output power. Table 2 summarize the simulation results for 4 different method of power control. Figure 8 shows the output power level for supply change from 0.3 to 2 V. From Figure 8, it can be understood that output power varies from 0.4 to 39.4 while PAE changes from 13.7 to 48.7%. CPO is 1.52 mW-percent. In this amplifier, bias voltage of M2 transistor can be used for power control. Figure 9 shows the output power versus bias voltage of M2 transistor variation form 0.6 V to 2 V. In Figure 9, output power and PAE change for 0.55 to 39 mW and 0.8 to 48.5%, respectively. In the Figure 10, PAE and output power of proposed PA are shown versus bias voltage of M2 transistor (V_{bias2}). Simulation results show that with M1 bias control form -0.15 to 0.7 V, output power changes from 0.5 to 46.3 mW and PAE changes from 4 to 49%. Furthermore, other conditions can be provided for output power control such that M2 bias voltage used. To get efficiency higher than zero minimum bias voltage must be 0.6 V. Also, bias of M1 can be used for controlled of output power. Simulation results in Figure 11 show that with supply voltage varying from 0.6 V to 2 V, output power changes from 0.4 to 39.4 mW and PAE from 6 to 48.7%. CPO is 1.64 mW-percent. Results indicate that M1 bias control provides a better merit. Also, Figure 12 shows PAE versus output power. It also shows that M1 bias control has a better condition comparing to other methods.

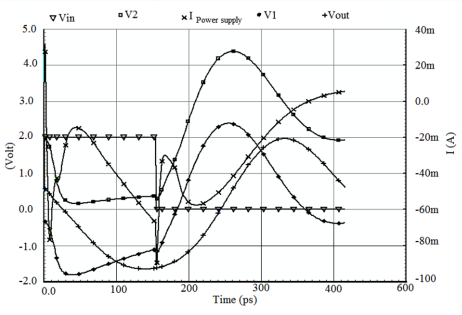

Figure 7. Waveforms for V1, V2, output voltage and power supply current for one period of input signal..

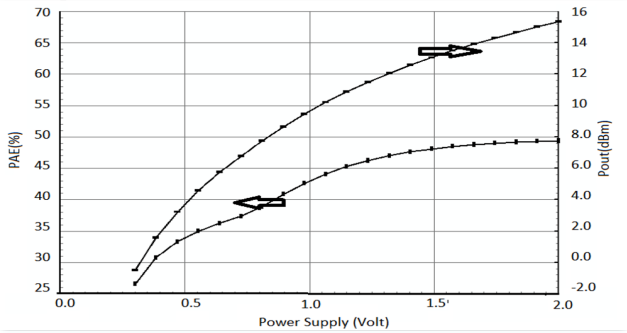

Figure 8. PAE and output power variations versus power supply.

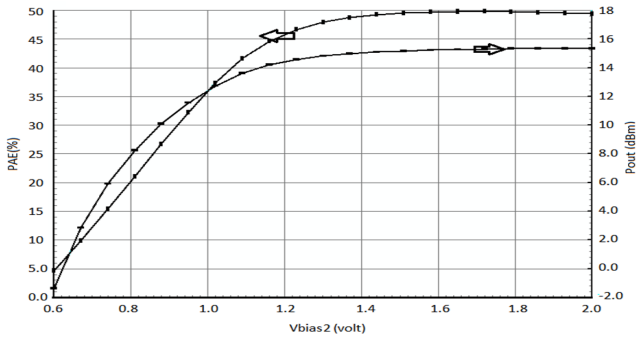

Figure 9. Output power and efficiency versus M2 bias voltage.

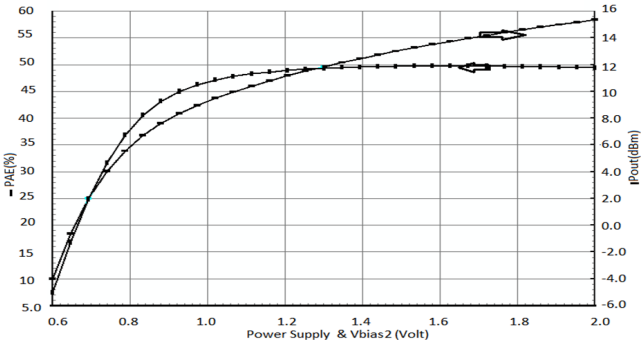

Figure 10. Output power and PAE versus power supply & Vbias2 of the proposed PA..

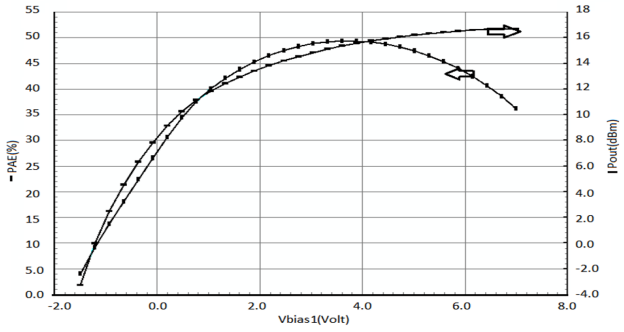

Figure 11. Output power and efficiency versus input signal DC offset (V_{bias1}).

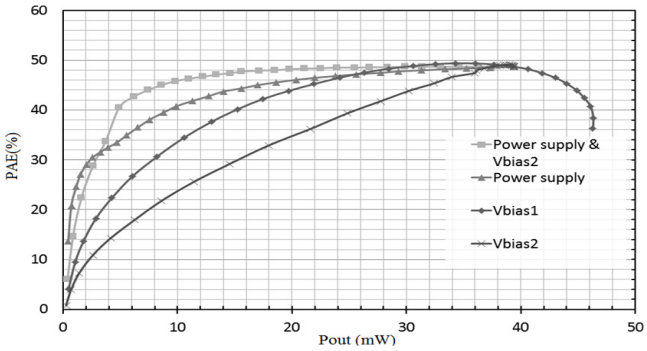

Figure 12. PAE versus output power for different power control lines.

Table 1. Component values for the proposed amplifier

Device	L_0	L_1	C_0	C_1	C_2	$W(M_1)$	$W(M_2)$
Value	3.1	2.6	7	0.9	0.7	320	560
Unit	nH	nH	pF	pF	pF	μm	μm

Table 2. A summary of simulation results for comparison between different power control lines

	Ave.PAE(%)	DR [P_{out}(mW)]	FOM
Power supply	39	39	1.521
V_{bias1}	38	45	1.710
V_{bais2}	37	39	1.443
Power supply & Vbias1	42	39	1.638

Figure 13 shows the layout of the amplifier. Excluding the pins, area is 0.6×1.6 mm^2. Figure 14 shows the output power and PAE versus different input signal amplitudes.

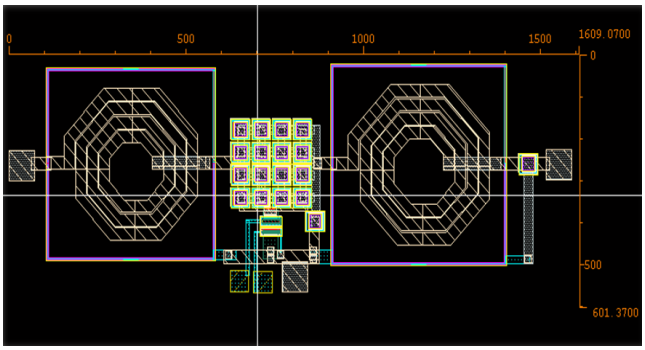

Figure 13. Layout of the proposed power amplifier.

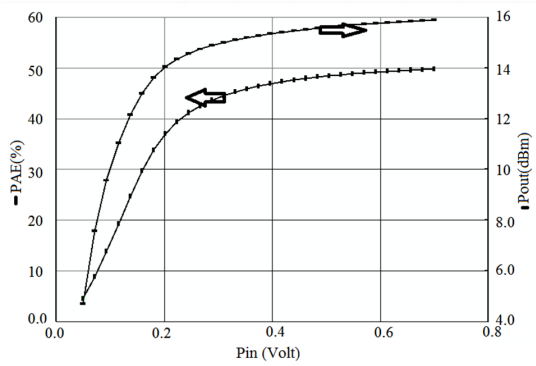

Figure 14. Output power and PAE versus input signal amplitude at 2.4 GHz.

In Table 3, a summary of some class-E amplifier specifications is provides. The proposed amplifier has better PAE. Also, PAE reported in[17] is higher but it has higher output power. In addition, control method in this work provides better control operation. Comparing to[11], all components of the proposed structure are on-chip. Especially on-chip inductors have lower quality factors while[11] used off-chip inductors with higher quality factor.

Table 3. Comparison table for reported different class-E power amplifiers and the proposed amplifier

References	Freq. (GHz)	$P_{out,Max}$(dBm)	PAE(%)	Vdd(V)	Tech. (μm)
[17]	2.4	0	55	0.5	0.13
[14]	1.8	33	31	3.3	0.18
[10]	2.2	18	35	1.6	0.18
[11]	1.7	31	58	2.5	0.13
Proposed (PA)	2.4	17	49	2	0.18

4. Conclusion

In this paper a class-E power amplifier is proposed working at 2400 MHz with 46 mW maximum output power and 49% PAE which is comparable with reported works. In the proposed amplifier, three methods investigated for output power control. With input transistor bias control, output power varies from 0.47 to 46.4 mW and PAE from 4 to 49%. To compare the performance of the power amplifier with voltage variation for different power control lines, CPO (Figure of Merit) is 1.72 mW-percent. The structure has been designed and implemented in 0.18 um CMOS technology. Some advantages of this design are fully- integrated structure, output power control and high efficiency.

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