# Simple CNFET Digital Circuit Design using Back-gate Voltages

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#### Abstract

Any real architecture designed only in the CNFET technology as a hopeful substitution of the silicon CMOSFET has not been developed because of shortage of self-assembly CNFET technology for designing complex CNFET structures. Therefore, for designing the real architecture in the current self-assembly CNFET technology, the development of a simple CNFET circuit structure forming all the digital function is required. This paper proposes a simple CNFET circuit structure using back-gate voltages to design the real digital architecture and to overcome the high fabrication cost of CNFETs and manufacturing variability and imperfection of CNFET technology. The function of the proposed CNFET cell is determined by the back-gate voltages, and the determined function is the same as NAND or NOR gate function. The simulation results present that the propagation delay time of the ISCAS85 circuits in a 32nm Stanford CNFET technology deploying the proposed CNFET cells is reduced by over 42% compared to the conventional CNFET cell in ultra-low voltage (0.4V).

Keywords: Back-gate Voltage, Carbon Nanotube FET, CNFET, CNFET Digital Circuit Design, Multi-function Logic

### 1. Introduction

Since Silicon MOSFET-like Carbon Nanotube FETs (CNFETs) have a one-dimensional band-structure for back-scattering restraint and a near-ballistic operation, CNFETs have been one of the hopeful substitutions for overcoming limit of the silicon MOSFET technology: the silicon MOSFET has scaling issues such as short channel effects, severe process variations, leakage power, high power density, and etc. Especially, the advantages of the CNFETs compared to Si-MOSFETs are as follows<sup>1-3</sup>. high on-current driving strength (although CNFET has a high-k gate oxide for leakage current reduction.), lower short channel effect, and higher sub-threshold slope.

However, a simple digital circuit (like ring oscillator and SRAM) has been implemented using CNFET technology, and any architecture only using the CNFET technology has not been presented. In addition, the carbon nanotube manufacturing at complex large circuits on a single substrate has not been developed until now. The reasons are that the fabrication cost of CNFETs is too high and CNFET technology has manufacturing variability and imperfection, and self-assembly technology for CNFET implementation has not been released yet to fabricate complex CNFET structures. Therefore, the development of a simple CNFET circuit structure forming all the digital function is required to design the complex digital circuits in the current CNFET technology. A few CNFET design methodologies for the real circuit systems have been researched, but the carbon nanotube structure is too complex or has many control signals<sup>4-8</sup>.

In this paper, we propose only one simple CNFET digital cell using CNFET back-gate voltages as function control signals. The function of the proposed CNFET cell is determined by the back-gate voltages, and the determined function is the same as NAND or NOR gate function, which means that any complex digital systems can be designed using the proposed CNFET cell although the current self-assembly technology is deployed.

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### 2. Background

This section presents the background of the carbon nanotube field effect transistor. Semiconducting single-wall carbon nanotubes is used to assemble CNFET electronic devices. The single walled CNFET substitutes the channel of a conventional MOSFET with carbon nantotubes as shown in Figure 1<sup>9-16</sup>, where a one-dimensional conductor can be obtained by rolling a sheet of graphite.

The carbon nanotubes can become either a metallic or a semiconductor by the angle (a chirality integer vector (n,m)) of the atom arrangement along the carbon nanotube. If the chirality integer n is equal to m or n-m is a multiple of three, the nanotube has metallic characteristics, whereas the nanotube has semiconductor characteristics. The CNFET device consists of drain, gate, source, and back-gate terminals. The conventional CNFET can be fabricated on a Si-substrate as shown in Figure 1(a), where the substrate can deployed as a backgate terminal making CNFET as dual-gate structures. Each CNFET includes one or more carbon nanotubes with semiconductor characteristics. The MOSFET like dual-gate structures have a conventional transistor characteristics, improved OFF state and sub-threshold slopes.



Figure 1. CNFET cross sectional and top view.

The number of nanotubes, pitch between nanotubes, chirality vector, and gate length are controlling parameters to control the CNFET current in the ON state<sup>1-2</sup>. As the ON or OFF state of the conventional MOSFFET is determined by the gate voltage, the CNFET is turned ON or OFF depending on the gate terminal voltage. In Figure 2, the ON current of the CNFET device using a 32nm N-type CNFET has been compared to those of the conventional Si-NMOSFET device. As shown in Figure 2, the CNFET drain current  $I_{DS}$  is saturated as  $V_{DS}$  increases and is increased as  $\mathrm{V}_{\mathrm{GS}}$  increases. The important thing is that the CNFET drain current is much greater than the Si-MOSFET drain current, where the MOSFET width is 64nm, and CNFET width is 6.35nm. Therefore, the CNFET technology can make a device size smaller in size (approximately an order of magnitude) compared to the Si-MOSFET.



**Figure 3.** 32nm N-type CNFET drain current as a function of  $V_{GS}$  for different  $V_{BG}$ , where the CNFET has (17,0) chirality integer vector, 2 nanotubes, and the width is 64nm.



**Figure 1.** 32nm N-type CNFET and a NMOSFET drain current as a function of: (a)  $V_{DS}$  for different  $V_{GS}$ , (b)  $V_{GS}$  for different  $V_{DS}$ , where the width of the CNFET is 64nm with (17.0) chirality integer vector and 2 nanotubes, the back-gate voltage is 0V.

Figure 2 (b) shows the characteristics of the N-type CNFET device in the weak inversion (sub-threshold) region, where the CNFET drain current in the weak inversion region is much higher than that of MOSFET. The simulation result of Figure 2(b) presents that sources of Si-MOSFET scaling limits such as the Drain-induced barrier lowering (DIBL) and Gate-induced drain leakage (GIDL) effects are almost disappeared, and the CNFET leakage current is much lower than that of the Si-MOFET.

# 3. Proposed Simple CNFET Digital Circuit

In Figure 3, the simulation result presents that the CNFET back-gate voltage increases the CNFET drain current by 30% compared to the CNFET device without  $V_{BG}$ . We utilize the CFFET  $V_{BG}$  characteristics for making a new simple CNFET digital circuit.

The proposed CNFET logic cell is shown in Figure 4 (a) consisting of two P-type CNFET, two N-type CNFET, two inputs, and two back-gates as function controlling inputs, where all the four CNFET devices have the same values regarding the number of nanotube, chirality integer vector, and etc. The key idea is that the function of the simple logic cell is determined by the back-gate voltage of each CNFET device. Depending on the back-gate voltages, if the N-type CNFETs are stronger than P-type CNFETs, the function is the same as NOR function, whereas if the P-type CNFETs stronger than N-type CNFETs, the function is the same as NAND function. Whenever the two inputs of the proposed cell are different each other, the CNFET cell output is influenced by the strength of P-type and N-type CNFETs.

For example, if a VDD signal is applied to a back-gate node of each P-type and N-type CNFET device, the N-type CNFETs are stronger than the P-type CNFETs as shown in Figure 2 (a). Therefore, the output function is a NOR function. On the other hand, , if a VSS signal is applied to a back-gate node of each P-type and N-type CNFET device, the P-type CNFETs are stronger than the N-type CNFETs as shown in Figure 2(b). Therefore, the output function is a NAND function. In addition, if the input A and B are connected each other, the function of the proposed CNFET cell is an inverter. Table 1 summarizes all the possible cell function depending on the back-gate voltage of each CNFET device.



**Figure 4.** A new Simple CNFET digital circuit structure: (a) proposed cell, (b) NOR function (with strong N-type CNFET) NAND function (with strong P-type CNFET).

Input A	Input B	Output (V <sub>pb</sub> =VDD, V <sub>nb</sub> =VDD)	Output $(V_{pb}=GND, V_{nb}=GND)$			
Low	Low	High	High			
Low	High	Low	High			
High	Low	Low	High			
High	High	Low	Low			
Function		NOR	NAND			
<i>If the input A and B are connected each other, the function is</i>						

 Table 1.
 Precision calculation of stego images

*If the input A and B are connected each other, the function is an inverter.* 



Figure 5. CNFET logic cell for low power consumption

The proposed gate can reduce the propagation delay of digital circuits by more than 50% due to the reduced number of stacks in the logic gate compared to a conventional NAND or NOR logic gate. Also, the reduced number of stacks can make digital circuits operated in low voltage region for ultra-low power application.

However, the power consumption of the proposed CNFET logic is much higher than that of the conventional NAND and NOR gate due to the increased static current from VDD to VSS (similar to the conventional pseudo NMOS logic gates). The proposed logic gate can be deployed more effectively only for high speed blocks rather than for the low power oriented blocks. To remove the static current effect on the proposed logic and reduce the power consumption, another CNFET cell for low power consumption has been proposed. Figure 5 presents the proposed low power oriented CNFET cell adding one N-type and one P-type CNFET device, respectively, where MN3 and MP3 CNFET device with an Enable signal are deployed to remove the static current of the high speed CNFET cell and reduce the power consumption at the cost of the delay increase of each CNFET gate.



**Figure 6.** Block diagram of digital circuits using the proposed high speed and low power CNFET cells



**Figure 7.** Proposed PLA architecture using the proposed simple CNFET logic cell

The key idea is that the Enable signal makes the CNFET cell operated whenever the inputs are asserted to digital circuits, and disconnects the CNFET cell if there are no inputs. However, the propagation is increased compared to the high speed CNFET cell.

Therefore, the final scheme is to use all the two proposed CNFET cells for considering performance and power consumption as shown in Figure 6. The high speed CNFET cell is placed on the longest critical path to reduce clock period, whereas the low power CNFET cell is placed on the non-critical path to reduce power consumption.

As shown in Figure 7, based on the aforementioned new CNFET logic cell, our goal is to extend the logic structure to a PLA architecture. In addition to the reconfigurable interconnects of conventional PLA architectures, reconfigurable back-gate voltage lines can be added to change the function type of each CNFET logic cell. Since the architecture deploys only one CNFET cell structure with the same parameters, the proposed PLA architecture would be simpler and cheaper than the conventional CNFET device.

Circuit	Circuit delay (sec)			Avg. Power Consumption (W)		
	Conventional logic gates	New logic gates	Reduction Rate (%)	Conventional logic gates	New logic gates	Increased rate (%)
C432	1.2602E-08	6.85E-09	45.61	7.24E-08	7.9307E-08	9.54
C499	2.9438E-09	1.70E-09	42.16	20.12E-08	2.2078E-07	9.73
C880	1.0077E-08	5.36E-09	46.80	14.01E-08	1.5321E-07	9.36
C1355	1.0572E-08	5.20E-09	50.86	19.43E-08	2.1029E-07	8.23
C1908	3.5330E-09	1.86E-09	47.43	26.31E-08	2.8299E-07	7.56
C2670	1.8220E-09	1.03E-09	43.21	32.24E-08	3.4993E-07	8.54
C3540	1.0795E-08	5.22E-09	51.66	88.12E-08	9.4932E-07	7.73
C5315	9.2415E-09	5.02E-09	45.70	110.01E-08	1.1811E-06	7.36
C6288	1.3903E-08	6.90E-09	50.36	154.43E-08	1.6405E-06	6.23
C7552	1.1442E-08	5.77E-09	49.53	138.31E-08	1.4738E-06	6.56

 Table 2. Simulation results for ISCAS85 benchmark circuits (VDD=0.4)

### 4. Simulation Results

The new simple CNFET cells have been designed and evaluated using ISCAS 85 benchmark circuits in 32nm Stanford CNFET at 0.4V supply voltages<sup>15</sup>. In the simulation, for considering performance and low power consumption, the longest critical paths are extracted using a commercial STA tool and the well-known algorithm of dual threshold voltage CMOS circuits<sup>17</sup>.

Table 2 shows the simulation results of ISCAS85 benchmark circuits with the conventional CNFET cells and the proposed simple CNFET cells. The circuit propagation delay and power consumption of the ISCAS85 circuits using the new simple CNFET cell have been compared to those using the conventional CNFET cells. In the simulation results, the circuit delay using the proposed CNFET has been reduced by over 42% compared to those using the conventional cells, and the power consumption is increased by over 10% compared those using the conventional cells. From the simulation results, it has been demonstrated that proposed CNFET cells can be used in high performance and ultra-low voltage system in the sub-threshold voltage region.

## 5. Conclusion

A new simple CNFET logic cell using back-gate voltages in a 32nm Stanford CNFET technology has been proposed to design the real digital architecture and to overcome the high fabrication cost of CNFETs and manufacturing variability and imperfection of CNFET technology. The simulation results present that the propagation delay time of the ISCAS85 circuits deploying the proposed CNFET cells is reduced by over 42% compared to the conventional CNFET cell in ultra-low voltage (0.4V). The effectiveness of the proposed gate and its utilization in PLA architecture will be investigated in the future, and the proposed CNFET cell will be a good solution for high performance in ultra-low voltage region.

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