Register Free Polar Codes Based Partially Parallel Encoder and Decoder Architecture

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Abstract

This paper presents about the partially parallel encoder and decoder architecture for polar-codes using register-free technique. In this paper, the folding transformation technique and register minimization technique are used for this architecture to reduce the circuit and timing complexity. In general, the polar codes are referred to a low complexity code to achieve the performance of channel carrying capacity in a binary-input memory-less channels. In the fully-parallel architecture, the hardware complexity is the major drawback which is high whereas in partially-parallel architecture the memory-sharing concept is utilized to overcome the complexity of hardware to attain the high throughput application. Thus, the temporary end results are saved within the registers instead of memories and multiplexers to manage the interlocking wires. Hence, the register aspect in polar code centered encoder and decoder architecture are eliminated. In an effort to support the information transmission efficiency stage, we get rid of the knowledge storage side (d-register) in stage-three and stage-four encoder and decoder method. Finally we reduce the 32 register elements for every data transmission process and mainly focus on the data storage and transmit function. Because the storage events are need to more time for data passing to one stage level to another stage.

Keywords: Partially-Parallel, Polar Codes, Polar Encoding, Register Free Technique

1. Introduction

Polar-coding is a capacity achieving code setting up method mainly for binary-input discrete memory much less channels. This can be done by the phenomenon of channel-polarization that every channel processes a flawlessly secure else a fully noisy channel as the code-length drives beyond over a collective channel built using a suite of N same sub channels[1]. 50% of power consumption can be reduced by parallel processing of two-input samples which reduces the frequency of operation by[2]. For small or adequate polar code, fault performance by the Cyclic Redundancy Check (CRC) supported Successive Cancelation List (SCL) decoding procedure is improved than the Successive Cancelation (SC) decoding process[3], which isn't appropriate for lengthy polar-codes owing to extreme hardware density. Linear block code with appropriate parameters can be used to perform block wise decoding of outer codes if there is not take into account, not necessary polar, as C_i^4. Path-search techniques for coding tree polar-codes are given as combined depiction of the SC, SCL, and SCS decoding algorithm. Integration of SCL and SCS, a new decoding process called the Successive Cancellation Hybrid (SCH). A semi-parallel-encoder based partial-sum update features as accessible architecture for SC decoding of polar-codes. This module uses Static Random Access Memory (SRAM) for storing, and uses a fixed data path. This design influences a multi-level quantization structure for Limb Lengthening and Reconstruction society (LLRs), reducing the memory usage and area[5].

In addition, Arıkan furnished a specific construction system for polar different understanding theoretic problems in an effective method then again, polar-codes require tremendous code lengths to strategy the capacity of the underlying channel[6]. Coding theorem by Shannon's

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proof for noisy channel is randomcoding method which is used to exhibit the presence of ability-reaching code structures without revealing any designated one[7]. In realistic implementations, the memory measurement and the usage of XOR-gates expand because code size increases. The polar-decoders is 8 times more than the successive cancellation decoder to increase the throughput of polar-decoding by an order of magnitude[8]. None of the previous works has deeply analyzedthe best way to the polar-code encoding effectively, although quite a lot of trade-offs are feasible among the latency and hardware difficulty. This design synthesized in a CMOS technology of 130nm for a parallel structure. Then again, the complex parallel structure has benefits of low latency and high throughput.The Polar Cosine Transform (PCT) algorithm used to divide the image into overlapping patches and then feature vectors are extracted from the patches. Hence, the polarization method is used in the image encryption and decryption[9]. Folding Transformation is a technique in which the number of butterflies in the same column is mapped into one butterfly unit.A pipelined parallel Fast Fourier Transform (FFT) architecture which has a lesser power consumption compared to serial FFT architectures[10]. Digital Signal Processor (DSP) operations are repetitive and periodic in nature. The life time chart specifies the life period of all variables in a single frame and the subsequent frames are computed in a periodic manner[11].

2. Existing System

Polar codes are newly proposed as the primary of low density of codes that obtains the memory less channel capacity for symmetric binary inputs. We built an Asynchronous State Machine (ASM) to change processing elements to manage the decoding through state transition procedure results low energy consumption. Our coding scheme also achieves the ability of the physically degraded receiver-orthogonal relay channel. Although, it reduces power and logical factors to reward a new low power system technique for Very Large Scale Integration (VLSI) technology. Moreover, the Partial Sum Network (PSN) for a SC decoder is viewed as polar-encoder. Considering that a polar-encoder mainly the inputs are taken from the buffer or memory which has greater bit-width, PSN is not suitable for planning a normal polar-encoding structure. The partially parallel encoder structure are designed for long polar code encoding efficiently. Thus the partially parallel architecture can be transformed by a four-parallelencoder structure for the 16-bit polar-code which is explained in detail. At first, fully parallel-encoding structure is converted into a folded-form and life-time analysis and the register-allocation are implemented to the folded-structure.

A fully parallel-encoding architecture was described for a length N of polar-code which has stages of n for $N=2^n$ and the coding complexity is $O(N \log N)$. For example, a 16-bit polar-code can be employed with 32-XOR gates and treated in 4-stages as shown in Figure.1.
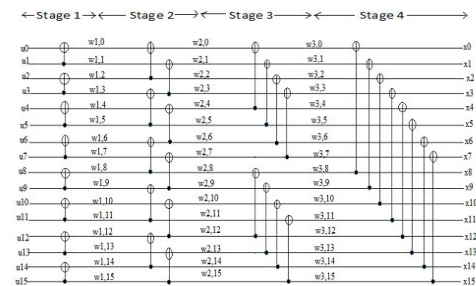

Figure 1. Fully Parallel Structure for a 16-bit Polar Code

In this architecture, the four samples are processed consequently in a cycle as per the folding-sets and register-allocation whereas the partially parallel structure as in Figure 2 processes the two samples in a given order as input and produces the two samples as output in a bit reversed order. Hence, the hardware complexity and power consumption can be reduced which is efficient for practical implementation of long polar codes.
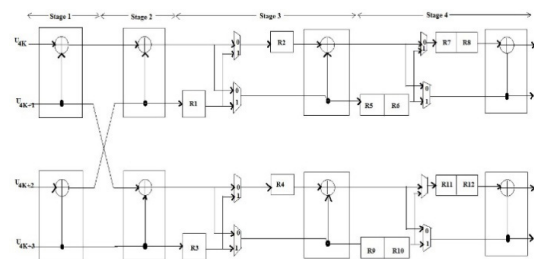

Figure 2. Partially Parallel Structure

3. Proposed System

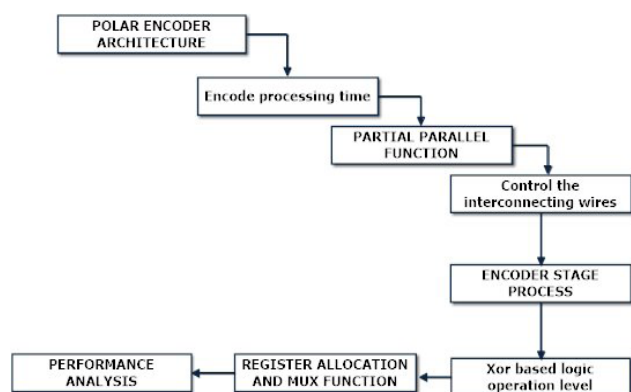The proposed architecture for implementing long polar codes is shown in Figure 3.

Figure 3. Proposed Architecture Diagram

Figure 4. Register Free Partial Parallel Structure

Table 1. Comparison Table

Terms	Existing System	Proposed System
LUT'S COUNT	140	120
FLIP FLOP OUNT	152	120
BIO COUNT	131	129
PATH DELAY TIME (ns)	1.972	1.884
POWER (mW)	101	99

In this proposed architecture, the polar code encoder architecture based on parallel form to minimize the logical gate count level and improve the encoding process time. Then, the partially parallel encoder architecture is implemented to achieve the trade-off between hardware cost and throughput and the temporary results are kept in the registers rather than multiplexers and memories to controlinterrelating wires. In the Encoder process, it consists of 4-stage process and each stage requires 4-bit input for encoder process. First stage to consist of XOR-gate function and second stage is to perform the inversed bit XOR-gate function level. Third and fourth stage process is consists of mux with register element and XOR based logic operation level which has more number of register elements. So, mainly focused on mux and register selection logical blocks. Register is used to hold the data in every clock cycle, but this model is consume more delay time, complexity level. So we implement the register free technique for polar code based data encoder and decoder architecture as shown in Figure 4. This operation is to improve the overall data transmission performance level.

4. Performance Analysis

In a large range the calculation of critical path done which is same for top and bottom leads to high clock frequency. Polar encoding is very appropriate to the Low-Density Parity-Check (LDPC) codes, since the number of ingoing messages to everyhandling units are even across the total clock cycles. From the synthesized results, it is found that the proposed system have reduction in the number of LookUp Tables (LUT's), Slices, Number of Slice Flip-Flop, Path-delay time and Power consumption when compared to the existing system as shown in Table 1.
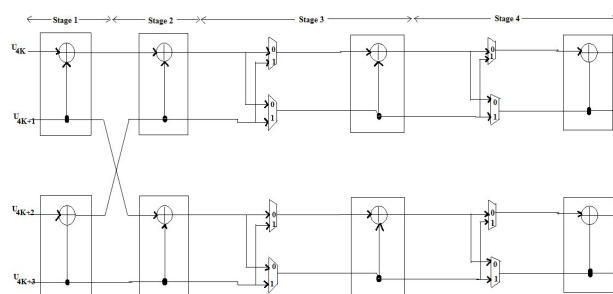
5. Conclusion

In this paper, the register free technique for partially parallel encoder and decoder architecture has been presented. Using this technique, the hardware complexity and delay time is reduced for partially parallel encoder and decoder architecture. Hence the 32 register elements are reduced mainly for the data storage and transmission. Thus, the proposed system suitable for real-time implementation of long polar codes.

6. References

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