ISSN (Print) : 0974-6846
ISSN (Online) : 0974-5645
Indian Journal of Science and Technology, *Vol 9(29), DOI: 10.17485/ijst/2016/v9i29/93237, August 2016*

Minimization of Area and Power in Digital System Design for Digital Combinational Circuits

R. Sivaraman and R. Parameshwaran

School of Computing, SASTRA University, Thanjavur, Tamil Nadu, India;
sivaraman77uma@gmail.com, paramu32@gmail.com

Abstract

This paper proposes enhanced parallel adder architectures with low power and reduced area. It includes, design of three different parallel adders such as Ripple Carry Adder (RCA), Carry Look ahead Adder (CLA) and Carry Select Adder (CSA). All three adders are designed in Gate Diffusion Interface (GDI) technique as well as traditional CMOS method. Adder is a basic common combinational digital circuit. Adders are important components in signal processing, image and video processing applications. So it is essential to have compact, low power adder design for these application fields. GDI based digital system design offers reduction in power consumption and area over head. When compared to traditional CMOS based design, GDI uses very less transistor to implement a function. The GDI and CMOS methods are taken in to account for the comparison of design parameters such as design layout, node to node delay, total power dissipation and speed of operation. All three parallel adders are designed in traditional CMOS as well as GDI method. The simulations are done using Microwind2 and DSCH2 analysis software tools and the results between those two types are listed below. This proposed adder circuits can be used in all high speed multipliers and filter designs where low power and reduced area is a major concern.

Keywords: Area, Combinational Circuits, Parallel Adders, Digital Design, Power

1. Introduction

The operation of addition is a rudimentary process for any audio and video processing system in digital domain. Addition is also used in control system applications to control. A quick and faultless behavior of a digital system design is significantly affected by the performance of adders. Adders are the most essential digital components in digital system design for their usage in filters, compressors and convertors. Hence upgrading potential of the digital adder design greatly improves the implementation of binary operations. The performance of any digital circuit is analyzed by its parameters such as speed, are and power. Adder circuits can be designed with many digital logics such as Pass Transistor Logic (PTL), CMOS, Dynamic CMOS, and Domino CMOS.

Out of above all logics, PTL is frequently used logic because of its low power consumption. In addition to power, PTL has some added advantages of maximum speed capacity, small area due to lower interconnects and very low power dissipation since its consumes low power. Even though PTL has many advantages over design, it has some draw backs by which it cannot be used for some applications. PTL has a problem that at each stage, the voltage levels are decreases due to the difference between high logic level and low logic level. GDI is an area reduction method can be used in all the combinational logic designs in digital system design. It is possible to imple-

*Author for correspondence

ment very complex logic function so easily with GDI method. It is worthy for the digital combinational design which needs low power consumption, reduced area, reduced complexity, less number of switching at nodes[1].

2. Primary Gate Diffusion Input Cell

The primary Gate Diffusion Input cell structure is shown in Figure 1. It can be carried out through twin tub process or else silicon on insulator process of CMOS fabrication technology. Figure 2 shows the GDI cell which is well matched with traditional CMOS process[1]. In traditional CMOS method, gate of PMOS and NMOS are shorted together where the input is to be given. And also both the power supply (Vdd) and ground (Gnd) connections are mandatory in traditional CMOS process. Yet in the case of GDI, any one of the global connections (Vdd, Gnd) is adequate to drive the circuit[2]. There are some differences between GDI and traditional CMOS which makes the GDI as a ruler. In traditional CMOS, Vdd has to be given in the drain terminal and Gnd has to be given in the source terminal. But in GDI, we can give logic inputs (logic 1, 0) in drain and source terminal. Basic GDI consist of only two transistors of PMOS and NMOS like traditional CMOS inverter design. From this basic GDI cell, wide range of digital combinational logics can be implemented[3-5].

Figure 1. Proposed GDI Technique.

Figure 2. Compatible with standard CMOS Process.

3. Parallel Adders

Full adder only adds three bits. If we want to add more bits, then parallel adders are the way to do it. Parallel adders are digital circuits which add more than three bits or binary strings. The functional diagram of structure of parallel adder is shown in Figure 3. In this paper, we have taken three parallel adders such as Ripple Carry Adder (RCA), Carry Look Ahead Adder (CLA) and Carry Select Adder (CSA) for design and implementation[6-8].

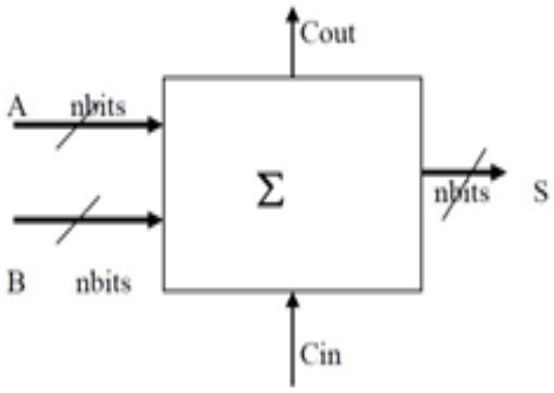

Figure 3. Parallel Adder.

4. Design of Adders using GDI Method

4.1 Full Adder

Full Adder (FA) is a very basic combinational digital circuit for addition operation. It takes three bits as input such as a, b and c in and gives s (sum) and co (carry out) as output. A full adder can be designed from Boolean expression or by cascading two half adders. In this design, full adder by two half adders is taken for building parallel adders. 'XOR', 'AND' and 'OR' gates are designed by Gate Diffusion Input method as shown in Figure 4-6 respectively. Full adder designed by GDI technique and its simulation with layout shown in Figure 7-9 respectively.

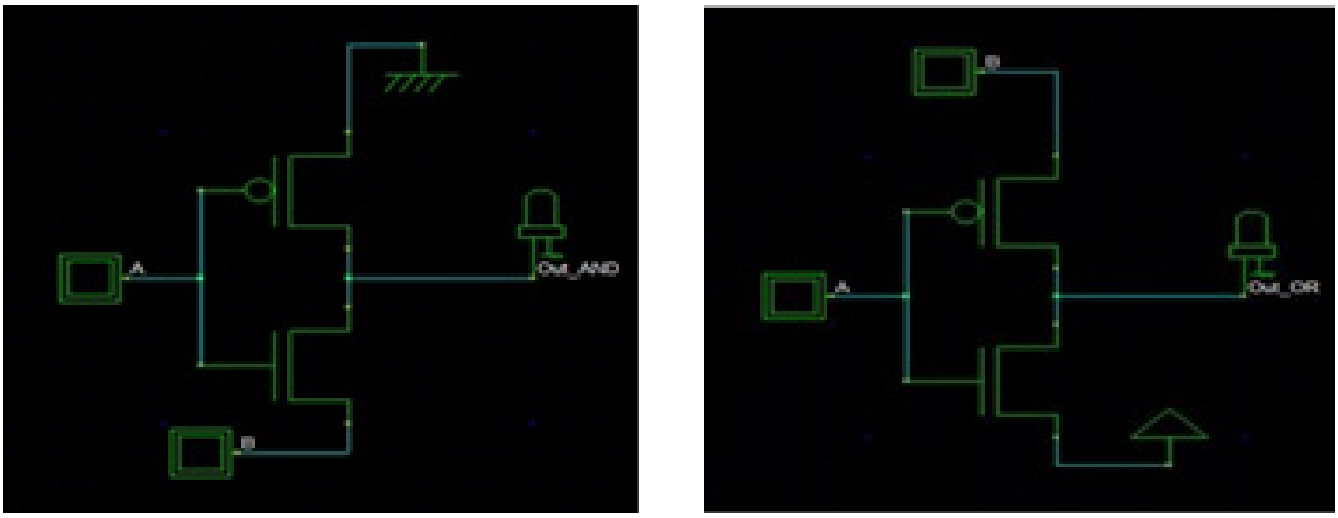

Figure 4. GDI design of AND, OR gate.

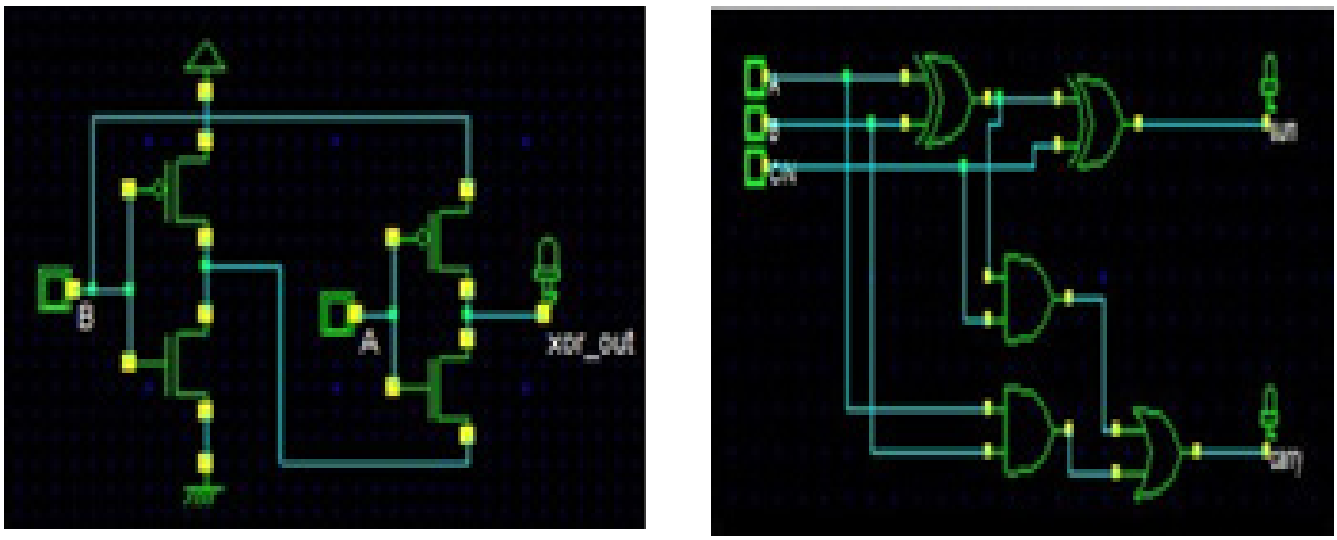

Figure 5. GDI XOR gate and Full Adder using Traditional CMOS.

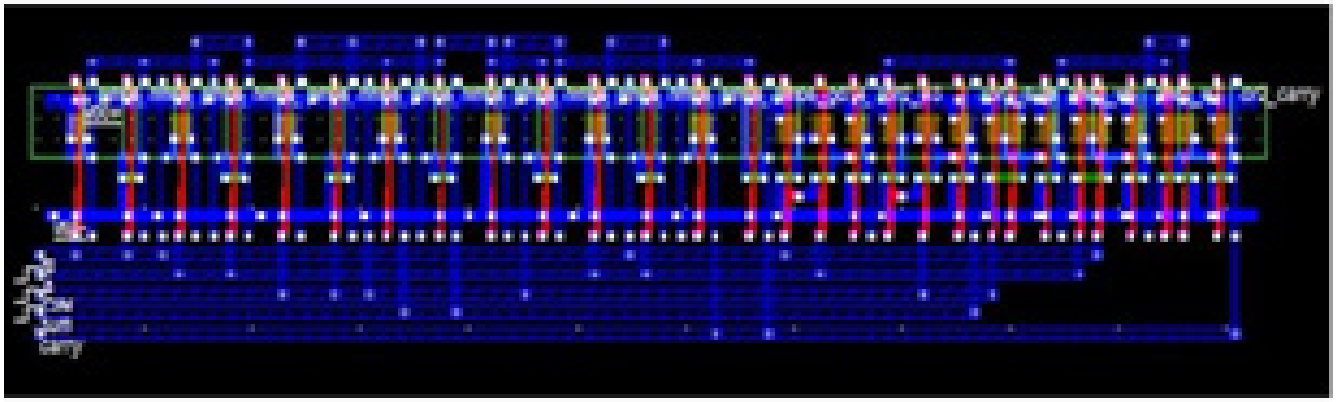

Figure 6. Traditional CMOS Full Adder Layout.

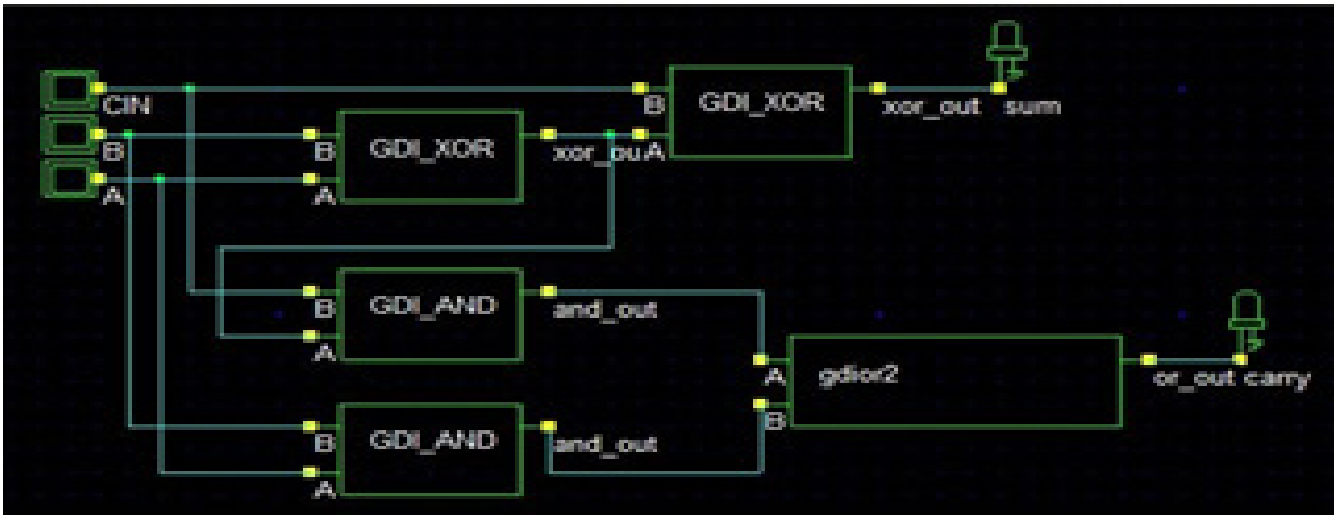

Figure 7. Full Adder using GDI Method.

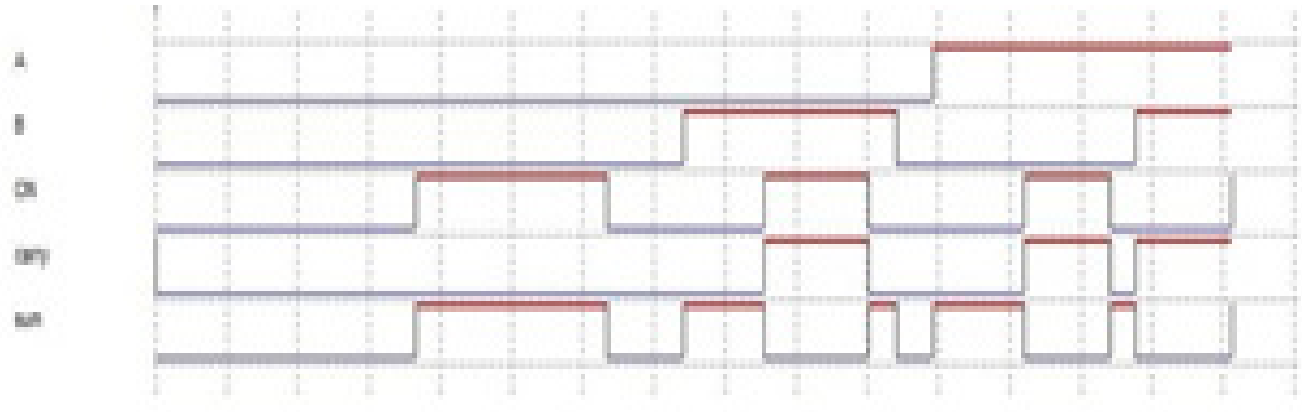

Figure 8. Full Adder simulation.

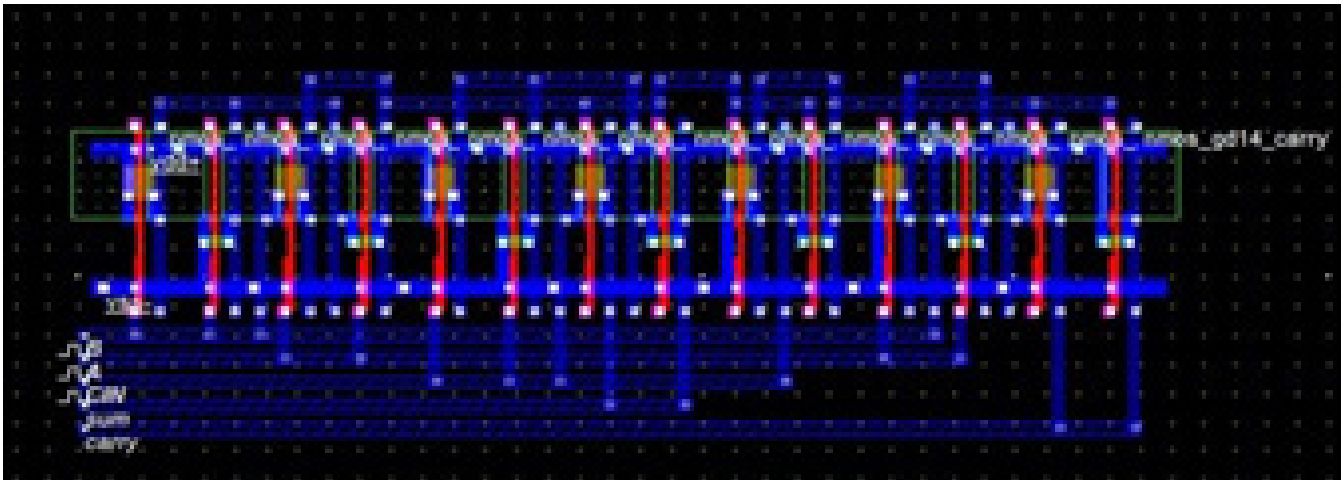

Figure 9. GDI Full Adder Layout.

4.2 Ripple Carry Adder

RCA is well known parallel adder that is designed by serially cascading several full adders as per requirements. Figure 10. Shows the ripple carry adder by GDI method and Figure 11. Shows the layout of it. This design uses four full adders connected in series. Each full adder adds three bits and produces sum and carry. Sum is directly taken out from the added block yet the carry is propagated from the first full adder block to final full adder block in order to generate the final carry. So after the computation of addition, we might have four sum values with one final carry.

Though this is simple method for n bits addition, it is not so efficient when large number of inputs is involved. The serious drawback of ripple carry adder is the delay of carry. As we explained before, carry is propagated from first block to final block since it generates delay in the performance of the design. Each stage of ripple carry adder is to wait for the carry which is to be generated from the previous stage.

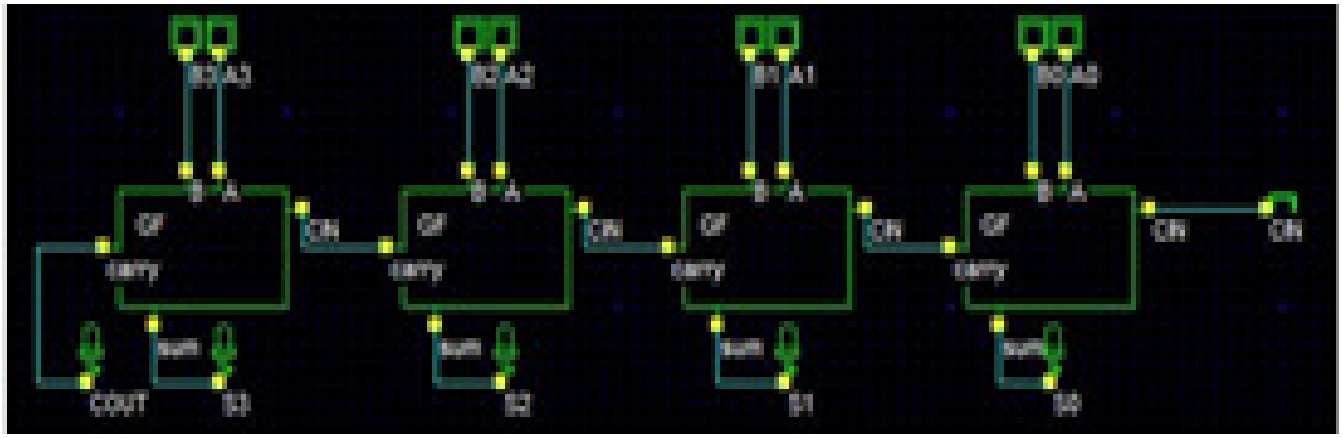

Figure 10. Ripple Carry Adder using GDI method.

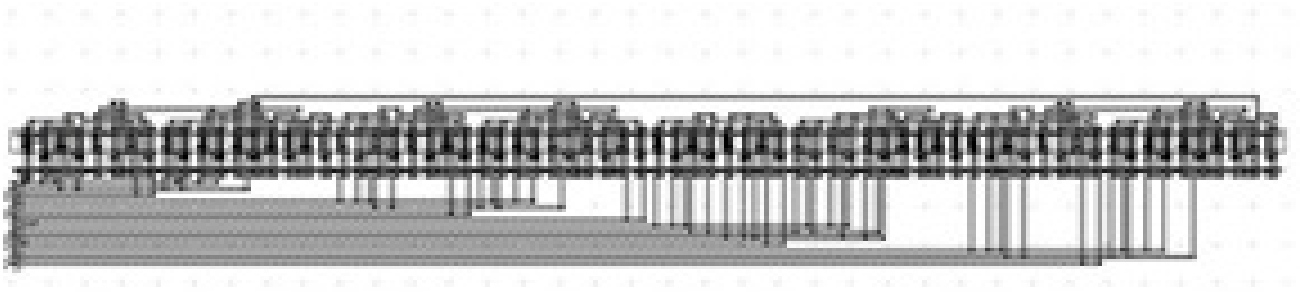

Figure 11. Ripple Carry Adder Microwind Layout.

4.3 Carry Look Ahead Adder

This adder overcomes the disadvantage of RCA such as propagation delay. A separate carry generation block is used here to generate carry for each state irrespective of previous state carries. This adder uses propagation and generation of carry to calculate carry signals in advance which reduces the propagation delay due to carry signal. Figure (12-13) shows the CLA design using GDI technique and its layout.

There are two sub blocks are designed in carry degeneration block named as propagation (Pi) and generation (Gi). Boolean expressions for Pi and Gi are expresses as,

pi = aixor bi (Propagate Carry),

gi = aibi(Generate Carry).

By applying these expressions in adder equations, we can get

si = pi xor ci-1,

ci+1= gi + pici.

So the carry generation will be:

c1 = g0 + p0c0

c2 = g1 + p1c1 = g1 + p1(g0 + p0c0) = g1 + p1g0 + p1p0c0

c3 = g2 + p2c2 = g2 + p2g1 + p2p1g0 + p2p1p0c0

c4 = g3 + p3c3 = g3 + p3g2 + p3p2g1 + p3p2p1g0 + p3p2p1p0c0

All the carry expressions are independent of previous stage carries. The well known expression of CLA is

ci+1= gi + pigi-1 + pipi-1gi-2 + ……. pipi-1….p2p1g0 + pipi-1 ….p1p0c0.

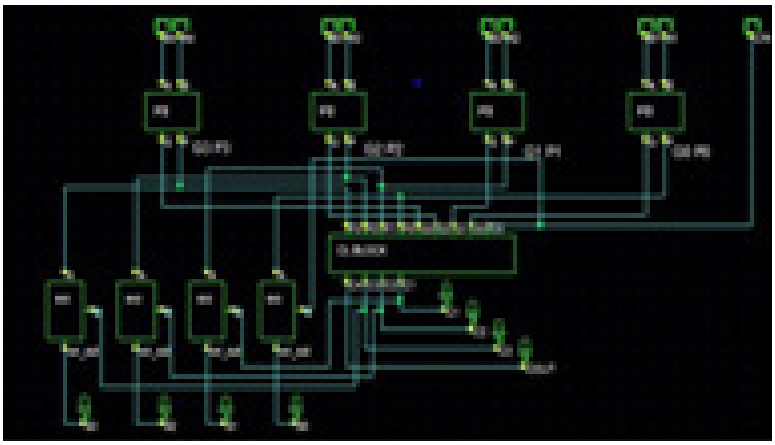

Figure 12. Carry look ahead Adder using GDI method.

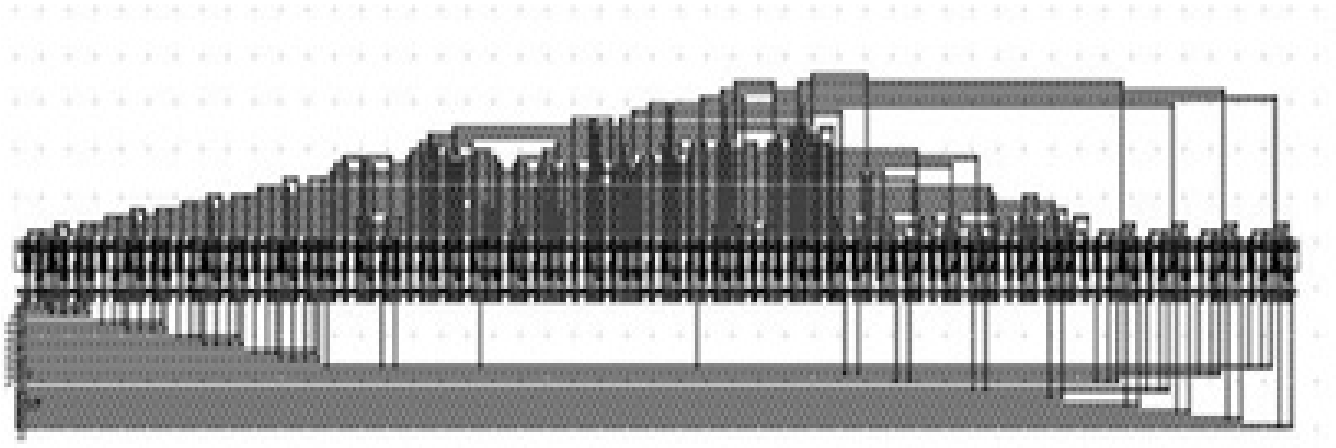

Figure 13. Carry look ahead Adder Microwind Layout.

4.4 Carry Select Adder

So far adders are generation results with respect to the initial carry which is to be given at first stage. Suppose if we want the results for both the carry inputs such as logic 1 and 0, for that carry select adder is proposed. The ultimate aim of CSA is to provide alternate results and solutions in parallel for both the carry inputs. So CSA has two RCA with multiplexer (MUX). Adders generate the sum and carry with respect to the inputs. Multiplexers are generating final results with respect to the initial carry. The following Figure (14-15) show the design of CSA using GDI method and its Microwind layout respectively. Table 1 explains the analysis carried over all the parallel adders proposed in this paper.

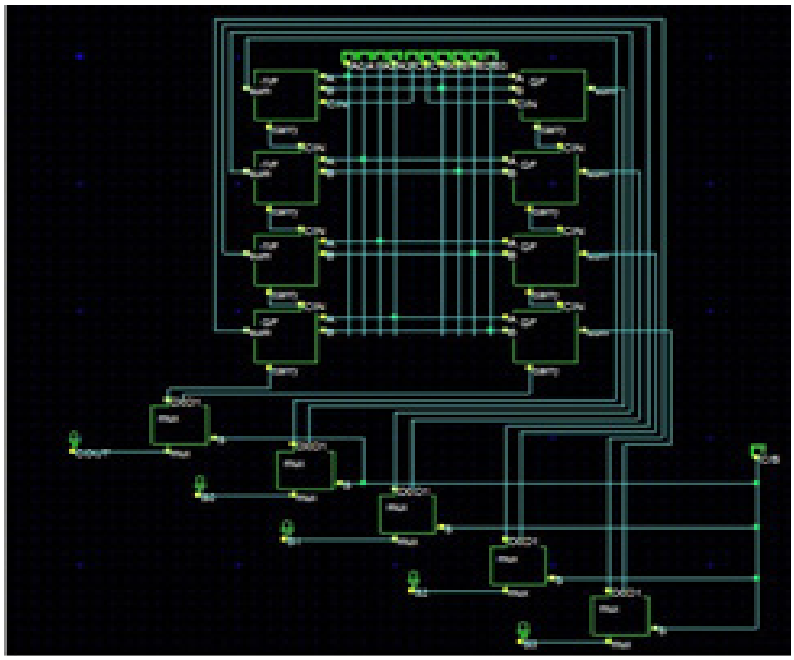

Figure 14. Carry Select Adder by GDI method.

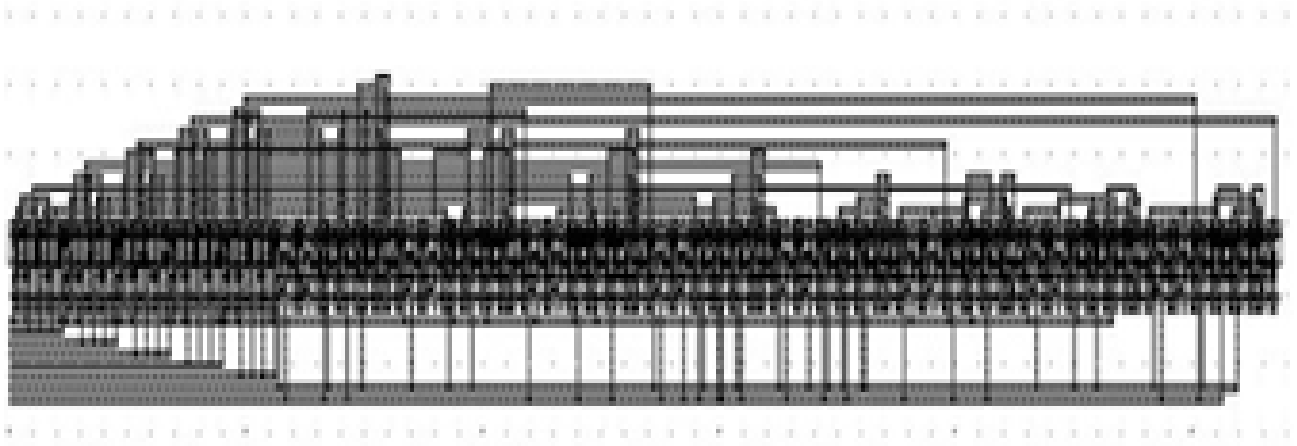

Figure 15. Carry Select Adder Microwind Layout.

Table 1. List of Adders using CMOS and GDI method.

Adders	Layout Size (um)	Power Consumption (uW)	No. of Transistors
CMOS Full Adder	16x5	9.425	42
CMOS Ripple carry Adder	64x18	26.045	168
CMOS Carry look ahead Adder	89x19	42.531	172
CMOS Carry Select Adder	160x22	58.737	351
GDI Full Adder	8x3	4.733	14
GDI Ripple carry Adder	32x9	13.970	56
GDI Carry look ahead Adder	43x15	29.326	72
GDI Carry Select Adder	61x17	36.381	120

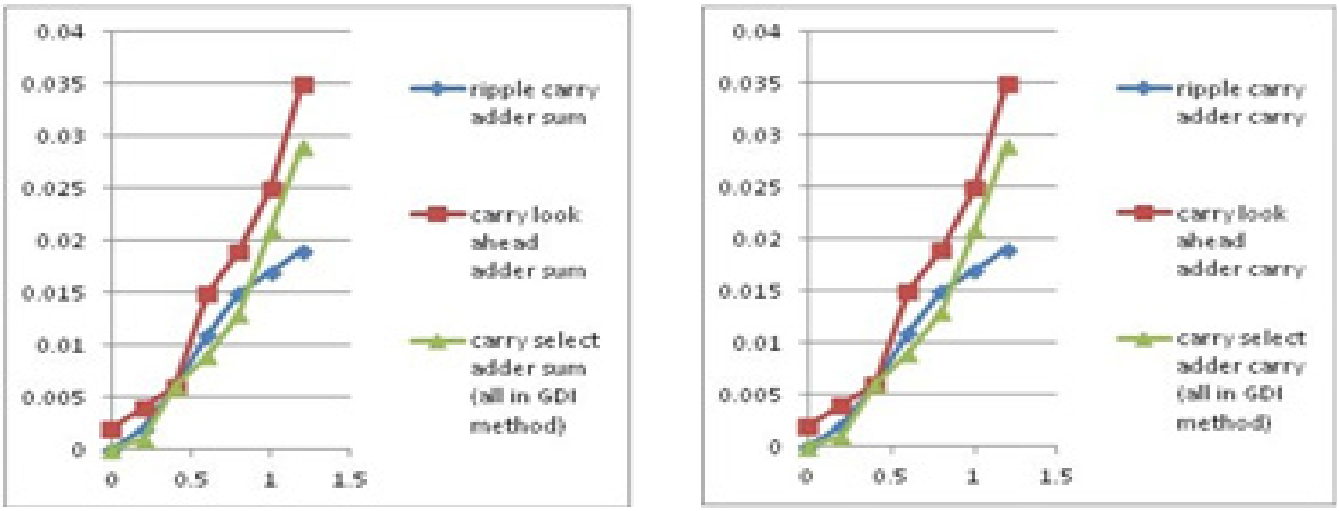

Figure 16. Power Dissipation in Sum and Carry of Parallel Adders.

5. Conclusion

Parallel adders are designed using GDI method and simulation results are verified using DSCH2 tool. With the help of Microwind 2 EDA tool, layout for each adder design is generated and power consumption, power dissipation, delay between nodes, transistor count and design area can be calculated and tabulated. Figure 16 shows the power dissipation in parallel adders. These GDI designed adders can be used in filters, ADCs, DACs and other signal, image and video processing fields. Thereby GDI method is a suitable digital combinational logic design method for low power consumption and low area applications.

6. References

1. Morgenstern A, Fish A, Israel I, Wagner W . Gate-Diffusion Input (GDI): A Power-Efficient Method for Digital Combinatorial Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems. October 2002; 10(5):566-581.
2. Umarani P. A High Performance Asynchronous Counter using Area and Power Efficient GDI T-Flip Flop. Indian Journal of Science and Technology. April 2015; 8(7):622–628.
3. Chandrakasan AP, Sheng S, Brodersen RW. Low- power CMOS digital design. IEEE J. Solid-State Circuits. Apr. 1992; 27:473–484.
4. Madhusudhan Dangeti, Singh SN. Minimization of Transistors Count and Power in an Embedded System using GDI Technique : A realization with digital circuits. International Journal of Electronics and Electrical Engineering ISSN. September 2012; 2(9):2277-7040.
5. Divya Gupta, Ravindra Prakash Gupta, Raju B.S.N. Analysis of Different CMOS Adders for Power Speed and Area. IJECT. Oct-Dec. 2011; 2(4):120-124.
6. Weste N, Eshraghian K. Principles of CMOS digital design. Reading, MA: Addison-Wesley.
7. Uyemura JP. Circuit Design for CMOS VLSI. Norwell, MA: Kluwer Academic, 1992. p. 88–129.
8. Baker RJ, Li HW, Boyce DE. CMOS circuit design, layout, and simulation. IEEE Press Series on Microelectronic Systems. 205–242.