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Design of an Efficient Low Power Multiplier: Combining Reversible and an Ancient Vedic Method Approach

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Abstract

Background: Multiplier is very important block which is being used in number of devices like DSP processor and microprocessors. Power consumption by multipliers decides the battery life of all these devices. Researchers are continuously striving for the multiplier which consumes less power but as the most dominant technology till now is CMOS, their efforts are not giving fruitful results due to physical constraints of CMOS device. **Methods:** In the proposed design used a reversible computing methodology and for circuit designing of multiplier used a QCA Cells. **Findings:** By combination of reversible computing and ancient Vedic method, a low power and high speed multiplier is proposed. **Improvements:** With this proposed technique, the Garbage outputs are reduced by 25%, numbers of gates are reduced by 5.40%, numbers of constant inputs are reduced by 6.89%, Quantum cost is reduced by 7.89% and TRLIC factor of this vedic multiplier is reduced by 16.89%.

Keywords: Reversible Logi, Quantum Cost, Urdhva Triyag Sutra, Vedic, VLSI

1. Introduction

Multiplication of two numbers is commonly used in almost every application. There are number of methods for multiplication of two numbers like ancient Vedas i.e. Vedic multiplication and addition. But this method is speedy and tricky to perform multiplication. Power consumption can be lowered in this multiplier by designing an efficient and facile architecture and maintain reversibility in that architecture. As Benett's proved that there will be almost no heat dissipation by applying logical reversibility in the circuit which is made up of reversible gates[1]. As per Landauer's principle if the circuit is made up of irreversible gate then it will lose $KTln_2$ of energy per bit erasure where K is Boltzmann's constant and T is temperature. Keeping this principle in mind reversible circuits are designed in which never lose information[1]. For maintaining such a logical reversibility there is need of synthesis of reversible circuit with reversible logic gates. Number of reversible gates can be seen in literature but based on some parameters these gates are selected[2]. This race of efficient multiplier was started by Maaz[3] by proposing a low power and high speed multiplier. Thapiyal and Srinivas contributed a lot in this era of designing multiplier with reversible feature[4, 5]. Rakshith also contributed in this era and proposed vedic multiplier architecture and with lesser TRLIC factor[6]. If a reversible gate is having N number of Qubits, then it is represented by $2^N * 2^N$ unitary matrix so the result of multiplication of multiplication of any arbitrary number of matrices is always unitary[7]. Nanotechnology is now under focus of researchers and it has huge potentials to supersede the projected limitation of CMOS. However, till now very little work has been reported on the capabilities of emerging technologies to perform computations. QCA is having huge potential as well as a prominent technology

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as it relies on novel design concepts. In this paper a novel architecture of vedic multiplier is mentioned by using reversible gates and this proposed multiplier is better in various parameters important for reversibility.

2. Methodology

2.1 Vedic Multiplication

Vedic multiplication is an ancient Indian technique for multiplication of two numbers. Vedic methods are speedy technique for doing multiplication. Nikhilam Sutra, Urdhva Tiryakbhaym and Urdhva Triyag Sutra[7] are different methods for multiplication. The proposed multiplier is based on Urdhve Triyag sutra algorithm. This algorithm was used for decimal number system in earlier days. It can also be applied to binary number system to achieve the required multiplication of two numbers. Let's take two number as 242 and 349. If both are multiplied by using this algorithm the result can be finding out by this algorithm as shown in Figure 1. As shown 2 is multiplied by 9 the result is 18 and pre-carry is 0 so 8 is result of final answer and 1 will be carry. In Figure 1(b) 9 is multiplied by 4 and 4 is multiplied 2 and added together respectively result is 44 and pre-carry is 1 so sum of both. is 45, 5 is final result and 4 is carry. So in this way this algorithm will be continued as shown in Figure 1 and the final result is 84458.

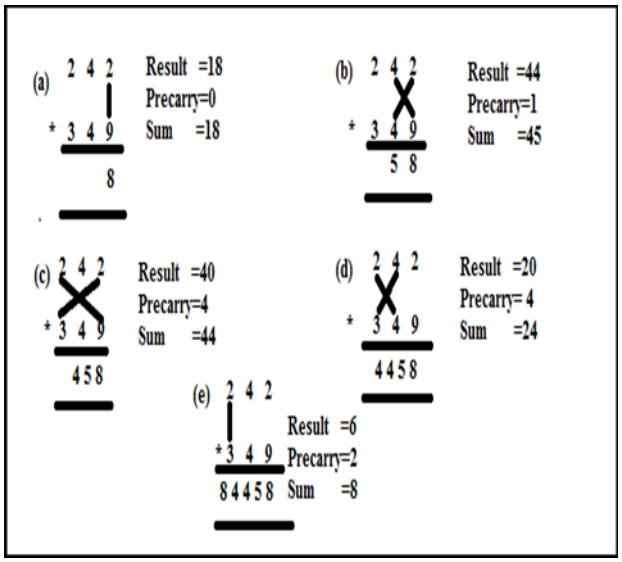

Figure 1. Urdhva-Triyag multiplication technique of two numbers (crosswise and vertically).

2.2 Urdhva-Triyag Multiplier (2*2 BIT)

2*2 bit multiplier is designed by using UT algorithm then this 2*2 UT multiplier will be used for doing 4*4 bit vedic multiplication. Let X and Y are two 2 bit numbers where X_0, X_1 and Y_0, Y_1 are representing their bits. The multiplication of these two bits' number is shown in Figure 2.

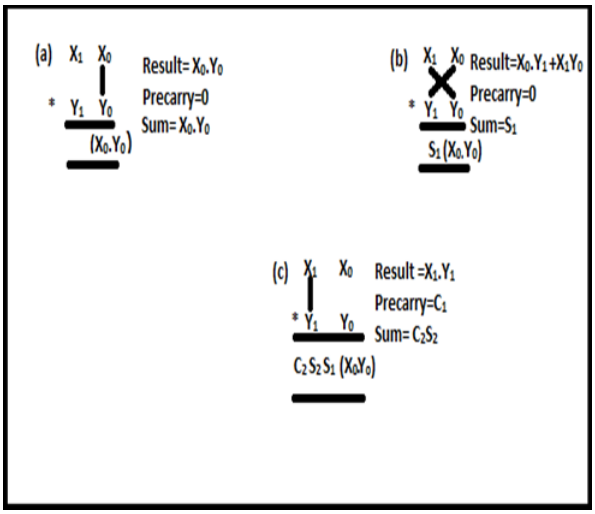

Figure 2. Algorithm for multiplication of two 2 bit numbers.

The block diagram for doing the hardware modelling of this algorithm is shown in Figure 3. In this 2 half adders and 4 and gates are used this can be implemented by using conventional logics and reversible logics. There are various benefits of using reversible logic over conventional logics in which the major benefit is low power dissipation.

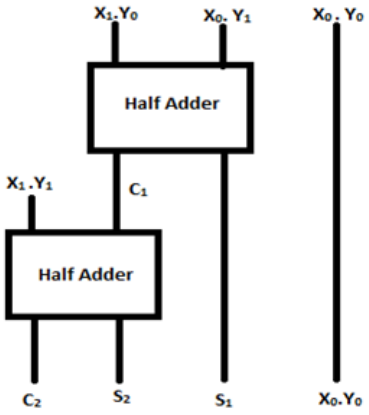

Figure 3. Block Diagram of 2*2 UT.

3. Reversible Computing

Reversible computing using reversible logic can be used in future for making computers with almost no heat dissipation. As present computers are not designed for

retaining information so they are irreversible computers which are designed by using conventional gates. Design's that retains information or doesn't lose information are reversible designs. If the designs are reversible Benett proved logical reversibility and proved that if network is made up of reversible logic gates, then zero power dissipation is possible[9].

In reversible logic the number of inputs are always equal to number of output and it always require bijective devices so after applying quantum mechanics in various application of computing this reversible computing emerged as new field. It leads to such kind of system in which without any power dissipation and with knowledge of past outputs, Future outputs can be easily predicted. For designing reversible circuits reversible gates are required and from past decade researchers are continuously searching for optimum reversible circuits in terms of constant inputs, garbage outputs, quantum cost, Number of gates and TRLIC factors[8] which are important parameters for describing optimum reversible circuits.

There are number of constraints for designing reversible circuits: -

- Fan-outs are not permitted in reversible logic circuits.
- Loops are not permitted.

For optimizing the reversible circuits following parameters to be taken care of: -

- They must have lesser number of garbage outputs which are defined as those outputs which does not contribute to realization of reversible logic design.
- They must have low quantum cost which are defined as the cost of permitive gates required to make reversible gates.
- The gates used to design reversible circuits should be as lesser as possible.
- Number of constant inputs should be as lesser as possible.

There are number of reversible gates which can be seen in literature [8].

3.1 Feynman Gate (CNOT gate)[8]

CNOT gate is 2*2 gate. The input vector is I(X, Y) and the output vector is O (P, Q). The outputs are given as P=X and Q=X xor Y. This gate act as copying gate and as fan-out is not permitted it can be used to provide fan-out in the circuit. IT's quantum cost is 1. CNOT gate is shown in Figure 4.

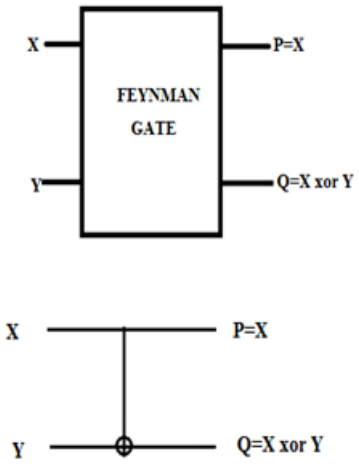

Figure 4. CNOT gate.

3.2 Peres Gate[8]

Peres gate is reversible gate with quantum cost of 4. The input vector is I (X, Y, Z) and the output vector is O(P,Q,R) then output is given as P=X, Q=X xor Y and R=X. Y xor Z. Peres gate is shown in Figure 5 Peres gate can be used as half adder if constant input 0 is provided at its third input Z as shown in Figure 6.

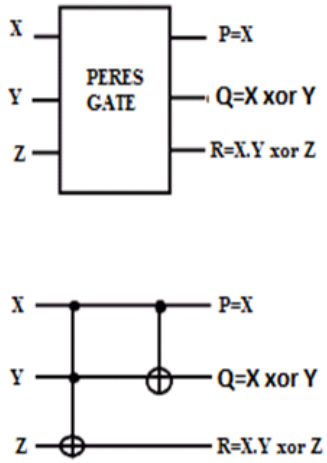

Figure 5. PERES gate.

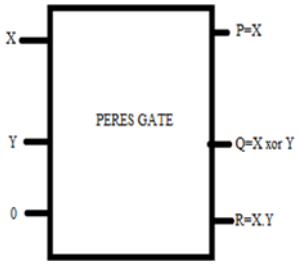

Figure 6. Peres gate as half adder.

3.3 Mux gate[8]

Mux gate [29] is 3*3 reversible gate with quantum cost of 4. Input vectors are given as I (X,Y,Z) and output vectors are given as O (P,Q,R). Outputs are given as P=X, Q=X xor Y xor Z and R=X'Z xor XY. It is shown in Figure 7.

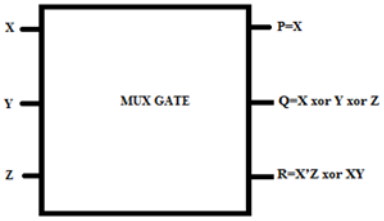

Figure 7. MUX Gate.

3.3.1 MUX gate as OR gate

MUX gate can be used as OR gate if it's input vector Y will be forced with constant input 1. It is shown in Figure 8.

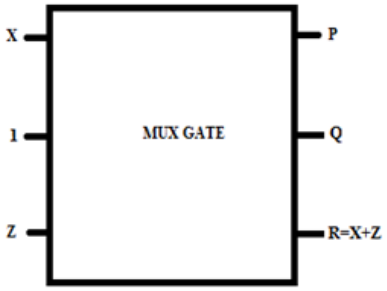

Figure 8. MUX gate as OR gate.

3.4 HNG Gate[6]

HNG gate is 4*4 reversible gate which can be singly act as full adder it is having quantum cost of 6. Input vector is I (W,X,Y,Z) and output vector is O (P,Q,R,S). outputs are given as P=W, Q=X, R=W xor X xor Y, S=[(W xor X) Y xor WX xor Z]. Hng gate is shown in Figure 9.

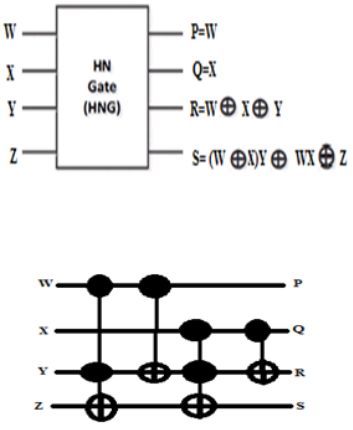

Figure 9. HNG gate.

3.4.1 HNG Gate as Full Adder

HNG gate can be singly act as full adder if input Z is forced to be 0. It is shown in Figure 10. Figure 10 Output R gives sum and S will give carry of inputs W, X, Y.

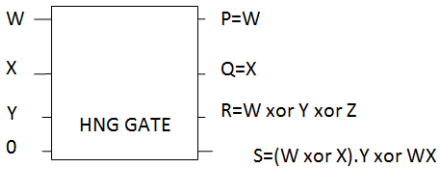

Figure 10. HNG gate as full adder.

4. Proposed Design

2*2 UT Reversible Multiplier

In 2*2 UT multipliers, primarily 2 gates i.e. Peres and Cnot gate are used. The Architecture of 2*2 UT is shown in Figure 11. In this architecture 5 Peres gate i.e. P_1, P_2, P_3, P_4, P_5 and 1 CNOT gate are used. The logical expression of Q_0, Q_1, Q_2 and Q_3 are mentioned below: -

$Q_0 = X_0 . Y_0$

$Q_1 = (X_1 . Y_0)$ xor $(X_0 . Y_1)$

$Q_2 = (X_0 . X_1 . Y_0 . Y_1)$ xor $(X_1 . Y_1)$

$Q_3 = X_0 . X_1 . Y_0 . Y_1$

Garbage outputs in this 2*2 UT is decreased by 4 as compared to the multiplier proposed by Rakshith as shown in Table 1.

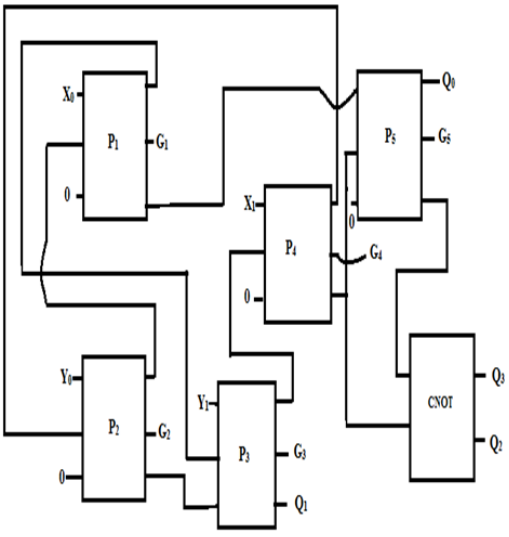

Figure 11. Architecture of 2*2 UT.

Table 1. Comparison of 2*2 UT

2*2 UT	Garbage Output
Proposed	5
[33]	9

So this 2*2 UT is better in terms of garbage output. This 2*2 UT will be used for implementing 4*4 UT. Simulation of 2*2 UT is shown in Figure 12.

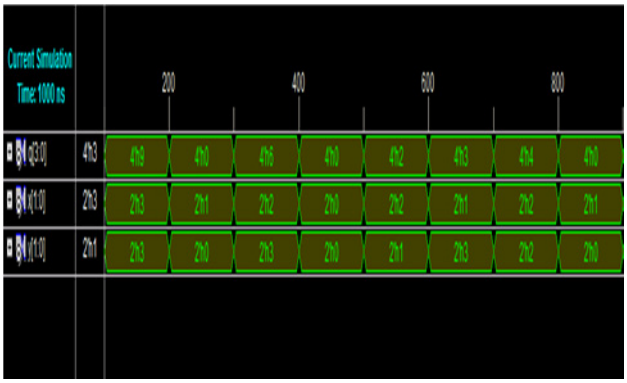

Figure 12. Simulation of 2*2 UT.

5. 4*4 UT Reversible Multiplier

4*4 UT multiplier is implemented by using stricture as shown in Figure 13. For implementation of this structure there is need of four 2*2 UT. Firstly input X_0 and X_1 will be multiplied with Y_0 and Y_1. Secondly input X_3 and X_2 will be multiplied withY_3 and Y_2. The middle one shows that two 2*2 bit multiplication with input X_2 ,X_3 & Y_0 ,Y_1 and X_0, X_1 & Y_2,Y_3 respectively. It gives the output of two 4 bit numbers having output R_0 to R_7. architecture of 4*4 UT multiplier is shown in Figure 14. The 4 bit Ripple carry adder is designed using reversible HNG gate and PERES gate. G is representing garbage outputs and X and Y are inputs as shown in Figure15. In the proposed architecture four 2*2 UT, two 4 bit ripple carry adder, one MUX as OR gate and two Peres gate as half adders are used.

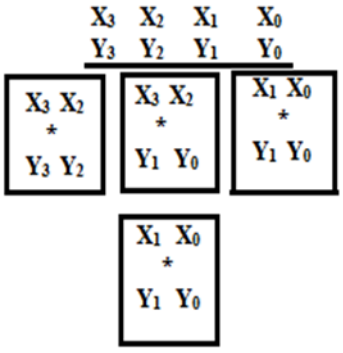

Figure 13. Structure of 4*4 UT multiplier.

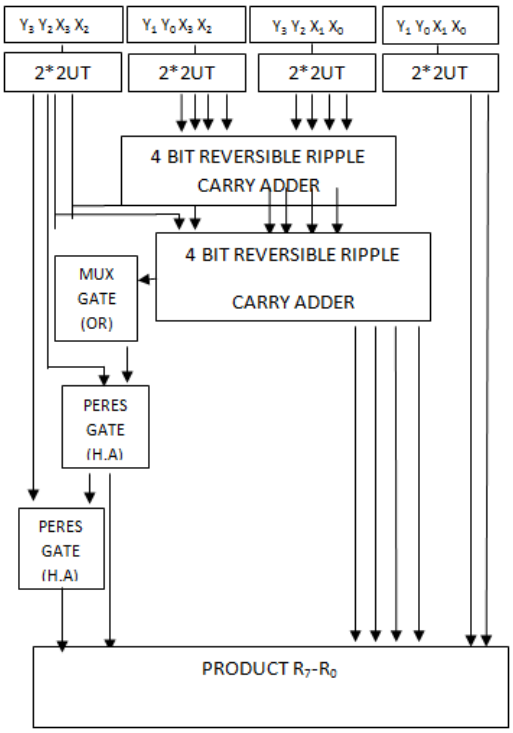

Figure 14. Architecture of 4*4 UT multiplier.

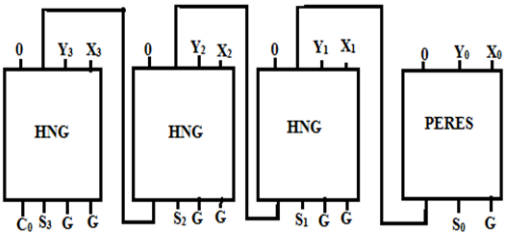

Figure 15. Design of 4 bit ripple carry adder.

6. Result and Discussion

The proposed architecture of multiplier is verified by software Xilinx 9.2i. Simulation of 4*4 reversible UT can be seen in Figure 16. This proposed multiplier is better than[7] in terms of number of gates used by 5.40%. Constant inputs are reduced by 6.89% as compared to[10]. After comparing with[10–13] garbage outputs are reduced by 25% and quantum cost are reduced by 7.89% as compared to [11] and [12].

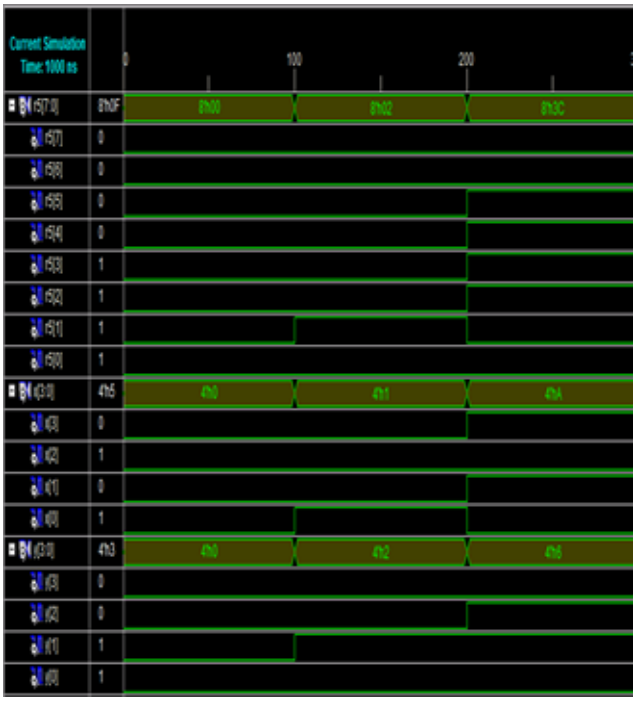

Figure 16. Simulation of Reversible 4*4 UT.

TRLIC means the total reversible logic implementation cost is computed by using equation (1) in which CI means constant input, NG means number of gates, QC means Quantum cost and GO means garbage outputs. Till now the multiplier proposed by [6] was better as compared to others as their TRLIC factor was 290 but the multiplier proposed in this paper is having TRLIC factor of 241. So it is efficient than[6] by 16.89%.

$$TRLIC = \sum (CI, NG, QC, GO) \quad (1)$$

As constant input, Number of gates, Quantum cost and garbage outputs are different cost metrics for circuit designed using reversible gates. TRLIC is sum of all those metrics. Our design is having least value of quantum cost, garbage output, constant inputs and Number of gates. The value of constant inputs achieved are 27, Number of gates are 35, garbage outputs are 39 and quantum cost are 140. The comparison of all metrics is shown in Table 2.

Table 2. Comparisons of Cost Metrics of Various Reversible Multipliers

Multiplier	Number of gates	Constant input	Garbage output	Quantum cost	TRLIC
Proposed design	**35**	**27**	**39**	**140**	**241**
6	37 (5.40%)	29 (6.89%)	62 (37.09%)	162 (13.58%)	290 (16.89%)
14	44 (20.45%)	44 (38.63%)	52 (25%)	160 (12.5%)	300 (19.66%)
11	52 (32.69%)	52 (48.07%)	52 (25%)	152 (7.89%)	308 (21.75%)
12	52 (32.69%)	52 (48.07%)	52 (25%)	152 (7.89%)	308 (21.75%)
13	52 (32.69%)	52 (48.07%)	52 (25%)	168 (16.66%)	324 (25.61%)
19	52 (32.69%)	56 (51.78%)	56 (30.35%)	208 (32.69%)	372 (35.21%)
20	53 (33.96%)	58 (53.44%)	58 (32.75%)	234 (40.17%)	403 (40.19%)
21	48 (27.08%)	52 (48.07%)	64 (39.06%)	244 (42.62%)	408 (40.93%)
22	64 (45.31%)	55 (50.90%)	56 (30.35%)	236 (40.67%)	411 (41.36%)
23	53 (33.96%)	58 (53.44%)	58 (32.75%)	286 (51.04%)	455 (47.03%)

7. Conclusion

The proposed architecture of multiplier is better as compared to other in terms of all cost metrics. It shows lesser power consumption as it is designed by using reversible gates. The Figure 17, 18, 19, 20 and 21 are showing the comparison of Number of gates, constant input, garbage outputs, Quantum cost and TRLIC factor for the proposed and other multipliers reported earlier. Quantum cost is the parameter which tells about the delay in the circuit as the quantum cost of this circuit is less by 7.89% in comparison with [43] and [42]. In this way lower quantum cost parameter will make it speedy. As the garbage outputs are very less so the power consumed in this proposed multiplier will be reduced by 25% as compared to[11, 12, 13, and 14]. Number of gates used and number of constant inputs are also reduced to high extent so this kind of efficient multiplier can be used readily in FFT chips for DSP processing as it will consume low power and will have very high speed as compared to other in literature.

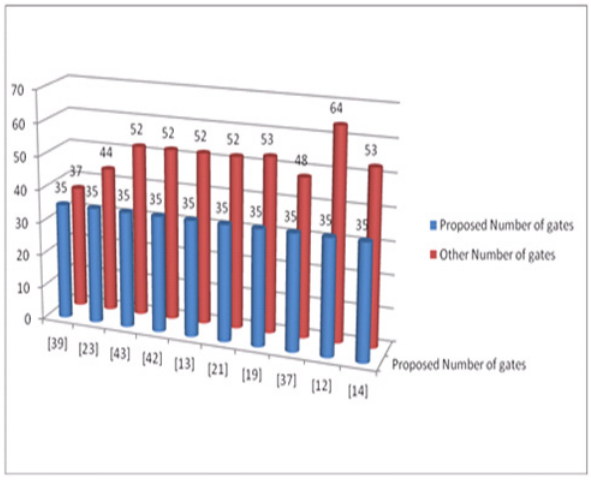

Figure 17. Comparision for Number of gates.

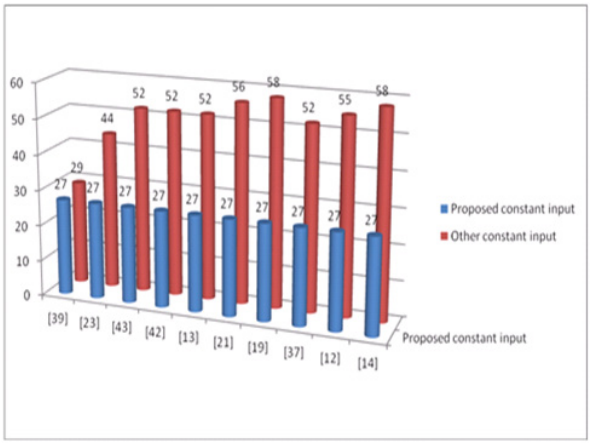

Figure 18. Comparision for constant input.

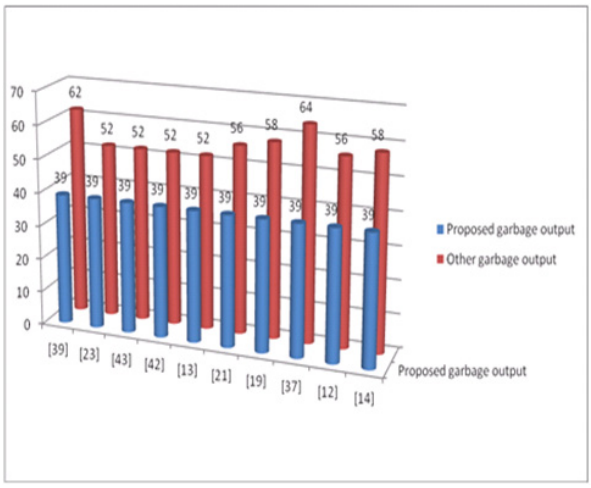

Figure 19. Comparision for garbage output.

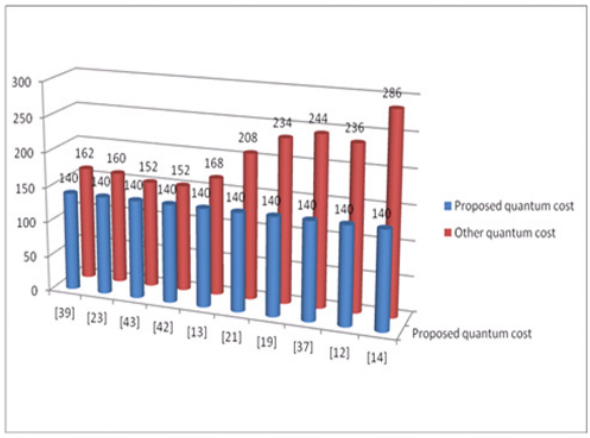

Figure 20. Comparision for quantum cost.

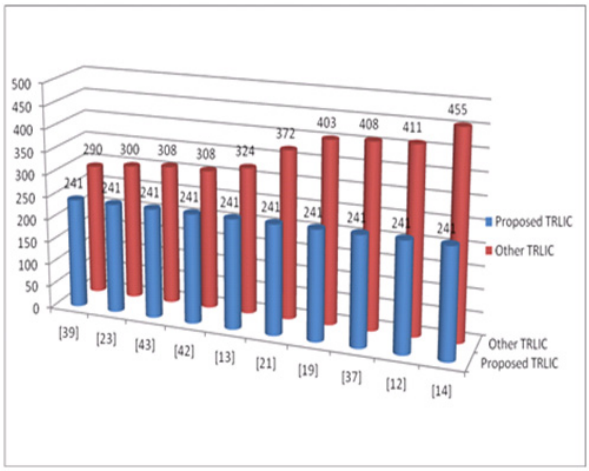

Figure 21. Comparision for TRLIC.

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