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Design and Implementation of Modified Russian Peasant Multiplier using MSQRTCSLA based Fir Filter

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Abstract

The aim of the current research work is to improve the architectural performances of digital filter. An efficient Multiplication and Accumulation (MAC) unit called "Russian Peasant Multiplier" is modified in this research work to alleviate the filter architecture. In proposed methods, switching activities of multiplier values has been validated by using only left shifters only, where as traditional Russian peasant multiplication has two shifters namely left and right respectively for validating multiplier values. Reduced Wallace Tree Generation (RWTG) method has been used to re-arrange the partial product results. Further Modified Square Root Carry Select Adder (MSQRTCSLA) has been incorporated into RWTG for performing accumulation operation of Multiplication. Proposed digital FIR Filter offers 45.61% improvements in hardware slices, 42.02% improvements in Slice Flip-flops, 22.36% improvements in sequential delay, 1.56% improvements in minimum input arrival time before clock, 0.86% improvements in maximum output required time after clock, 19.52% improvements in dynamic power and 18.32% improvements in total power consumption than traditional Russian peasant multiplication based digital FIR filter. In future, proposed MAC based FIR filter architecture will be absolutely suited to Software Defined Radio (SDR) and Orthogonal Frequency Division Multiplexing (OFDM) based data communication applications for improving hardware speed and power consumptions.

Keywords: Reduced Full Adder, Reduced Gate Level Logic, Reduced Half Adder, VLSI based filter design, Wallace Tree Generation

1. Introduction

Finite Impulse Response (FIR) filter have been tremendous and swift growth in various wireless communication applications. Convolutions, Correlations, Frequency Transformation techniques are the crucial digital signal processing operations. Among those operations, FIR filter plays a major role in Software Defined Radio (SDR) and Orthogonal Frequency Division Multiplexing (OFDM) based communication system. Large endeavours have been suggested the direct form FIR filter to filter the unwanted signals. The relationship of input-output Linear Time Invariant (LTI) System is represented as in equation (1),

$$y_{out}(n) = \sum_{p=0}^{N-1} Coeff_{\ p} x_{in}(n-1) \quad (1)$$

Where, Y_{out} (n) represents the output samples, X_{in} (n) represents the input samples, $Coeff_p$ represents the filter coefficients and N is the order of the filter or length of the filter. As per the equation (1), signals are filtered at finite impulse response (represented in mathematical form). X_{in} (n-1) is the delayed version of input samples. Hence, different values of coefficients are multiplied with delayed version of input samples in every clock period. The design of FIR filter model is based on sequential design. Therefore, digital or direct form FIR filter is also named as "Sequential FIR filter". Software Defined Radio (SDR),

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Discrete Wavelet Transformation (DWT) and Discrete Cosine Transformation (DCT) require both Low Pass Filter (LPF) and High Pass Filter (HPF) to process the data over high frequency and compress the image by level by level respectively. Levels of Coefficient values decide the types of FIR filter (Low Pass or High Pass). Based on this requirement, Reconfigurable FIR filter has been introduced in the past.

The order of FIR filter is fixed in case of Direct Form FIR Filter. In order to reduce more noise/distortion and improve the spectral containment, more number of taps is necessary in direct form FIR filter. But, computational delay has been raised rapidly with increasing the number of taps due to MAC functions. Hence, synchronous and pipelined structure of MAC unit is essential for reducing computational and sequential delay. In order to attain this requirement, Modified Russian Peasant Multiplier (MRPM) using Modified Square Root Carry Select Adder (MSQRTCSLA) based MAC unit is designed in this paper. Further, designed MAC unit has been incorporated into 8-tap digital FIR filter for realizing the performances of developed MAC unit and improving the digital architectural performances of FIR filter.

The main aim of Very Large Scale Integration (VLSI) System design is to reduce the hardware complexity in terms of Slices, Look Up Tables (LUTs), Memories & Registers and improve the speed of the processor. Ripple Carry Adder (RCA) is the one the basic VLSI based adders in which Carry Propagation Delay (CPD) affects the performances of adder. To reduce the CPD delay, different types of enhanced and optimized adders (Carry Skip Adder (CSKA), Carry Select Adder (CSLA), Carry Save Adder (CSA), Sklansky Adder, and Parallel Prefix Adder (PPA)) are introduced and developed by large endeavours. CSLA adder has parallel data flow structure[9]. It reduces the 25% of gate count than CSKA. Also gate count of CSLA[9] is modelled as $5n+\log^2 n/2$. Proposed parallel adder[9] offers 24.3% speed improvement than traditional CSKA. Traditionally, CSLA has dual RCA sets for performing Half Sum Generation (HSG) and Full Sum Generation (FSG). Both HSG and FSG have critical computation paths. Gate-level modifications have been made in HSG and FSG blocks for reducing the computational path. Developed HSG and FSG models have only combined Full Adders (FAs) and Half Adders (HAs)[7]. The same CSLA architecture has been further enhanced by using Carry Generation when input carry 0 (CG-0), Carry Generation when input carry 1 (CG-1) and Carry Selection (CS) unit[5]. When compared to design of[7], CS & CG based CSLA gives best performances in area-delay and power.

Multiplication and Accumulation (MAC) unit play a vital role in every digital signal processing operation. Three main operations are involved in MAC functions to find the multiplication results such as Partial Product Generation (PPG), Wallace Tree Reduction (WTR) and Final Adder Unit (FAU). Reduced Wallace Tree Reduction (RWTR)[10] method has been designed with the help of FAs and HAs. Finite Impulse Response (FIR) filter require MAC unit to find frequency path of Low Pass Filter (LPF) and High Pass Filter (HPF). Reconfigurable FIR filter has been designed by using Russian Peasant Multiplier (RPM)[1]. Carry Select Adder (CSLA) with Sklansky Adder is used in the design of[2] for performing addition operation of MAC unit. It offers 30.9% reduction of area than traditional CSLA. Further to improve the architecture, some modifications are made in CG block of CSLA architecture.

Reconfiguration techniques make a productive modification on existing configurations without alter any functionality with improving efficiency in various aspects. Reconfigurable FIR filter have been tremendous and swift growth in current trends of wireless communication based applications. Vertical-Horizontal Binary Common Sub-expression Elimination (VHBCSE) technique[3] is used to design the reconfigurable FIR filter. Multiple Constant Multiplication (MCM) technique is used in [5] along with BCSE.

2. Digital IIR and FIR Filter

The architecture of 8-tap direct form FIR filter is illustrated in Figure 1. It consists of delay elements, Multipliers and Accumulators for performing the filtering process at finite impulse durations. Register unit is used to store and retrieve the intermediate data. Program Shift Counter (PSC) is used to pre-allocate the data flow assignment. Multiplication and Accumulation (MAC) unit of Figure 1 decides the duration of finite impulse responses. From Figure 1, it is clear that an efficient multiplier and accumulator structures are required for implementing the digital FIR filter. The architecture of Infinite Impulse Response (IIR) filter has been illustrated in Figure 2. Like FIR filter, IIR filter has both MAC and delay units to perform the LPF or HPF operation at infinite impulse duration. Mathematical expressions for both FIR and IIR filter is represented in equation (1). Based on filter

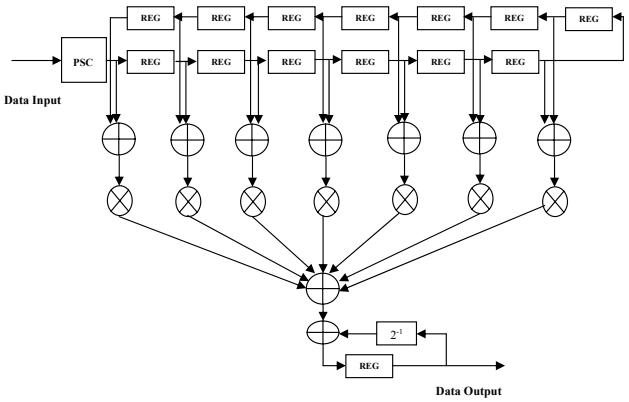

Figure 1. Architecture of 8-tap FIR filter.

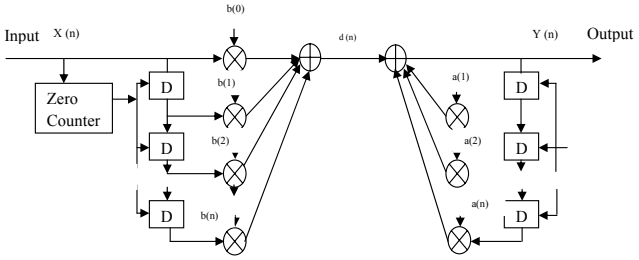

Figure 2. Architecture of IIR filter.

coefficient values, duration of permitting and blocking frequency ranges should be determined in both LPF and HPF filters.

3. Modified Square Root Carry Select Adder

Ripple Carry Adder (RCA) is one of the best VLSI based adders in which Carry Propagation Delay (CPD) affects the performances of addition operation. In order to overcome this problem, Carry Look-ahead Adder (CLA) has been introduced in the past. In CLA, logic gates (XOR, AND, OR) are used to produce generate and propagation signals. Hence, it executes in a parallel manner. However, it reduces the performances due to utilizing more number of logic gates. From above sequence, it is clear that an efficient adder must meet the following requirement.

- Less Gate Count (in terms of less gates & hardware)
- High Speed (in terms of low combinational and sequential delay)
- Lower power consumption
- High Frequency

Carry Save Adder (CSA) and Modified Carry Save Adder (Square Root Carry Select Adder) have above requirement with pipelined and parallel architecture. Traditional CSLA architecture has dual RCA and Multiplexors for providing 'n' bit addition process. But, dual RCA should not help to improve the architectural performances; hence one of dual set RCAs has been replaced by Binary to Excess 1 Converter (BEC) circuit. Hence updated CSLA circuit is named as "BEC based SQRT CSLA".

In this paper, Gate counts of FA and HA has been realized and re-designed with reduced number of logic gates. Hence, modified designs are named as "Reduced Full Adder (RFA)" and "Reduced Half Adder (RHA)" respectively. RFA uses only 9 gates whereas traditional FA uses 13 gates and RHA uses only 4 gates whereas traditional HA uses 6 gates. The structure of RFA and RHA has been illustrated in Figure 3 and Figure 4 respectively.

16-bit BEC based SQRT CSLA has 4 groups and each has combination of FA and HA circuits. In the developed design, RFA and RHA have been incorporated in the place of FA and HA of group structures. Hence, it helps to improve the performances in terms of less slice

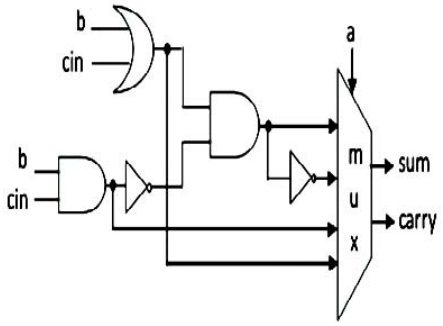

Figure 3. Structure of Reduced Full Adder

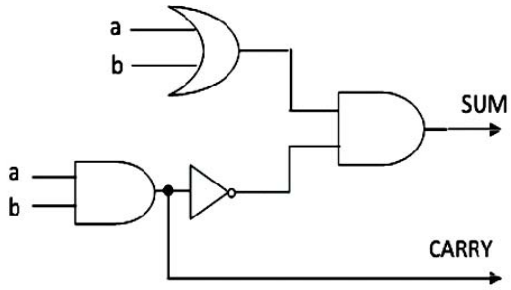

Figure 4. Structure of Reduced Half Adder.

& memory utilization, delay and power consumption. The comparison of gate count for both traditional BEC based SQRT CSLA and MSQRTCSLA has been made in Table 1.

4. Modified Russian Peasant Multiplier

Russian Peasant Multiplication (RPM) is the best multiplication algorithms which based on "Multiply-Divide" principle. In the perspective of digital implementation, left-shifters and right-shifters are used to multiply and divide 'n' bit binary data. Hence, shifters based digital circuit is designed to perform the multiplication operation by using Russian Peasant Multiplication algorithm. Developed Digital Multiplication called as "Digital Russian Peasant Multiplier (DRPM)". General Multiplication has three stages as follows,

- Partial Product Generation (PPG) to generate the partial products
- Wallace Tree Reduction (WTR) to re-arrange the results of partial products
- Final Addition Unit (FAU) to add final outcome from WTR

In DRPM, only one shifter is used to provide the PPG results. To re-arrange the PPG results, Reduced Wallace Tree Generation (RWTG) pattern has been developed. In final stage of RWTG, an efficient accumulation structure is required for implementing 'n' bit addition operation. In order to fulfil this requirement, developed MSQRTCSLA has been incorporated into DRPM multiplier. Hence, Proposed Multiplier architecture is named as "Modified Digital Russian Peasant Multiplier (MRPM or MDRPM). The structure of MDRPM has been illustrated in Figure 5.

Table 1. Gate count for both traditional BEC based SQRT CSLA and MSQRTCSLA

Traditional BEC based SQRT CSLA		MSQRTCSLA		Percentage Reduction
Group-2	39	Group-2	31	20.51%
Group-3	58	Group-3	45	22.41%
Group-4	77	Group-4	59	23.37%
Group-5	96	Group-5	73	23.95%
Total	270	Total	208	22.96%

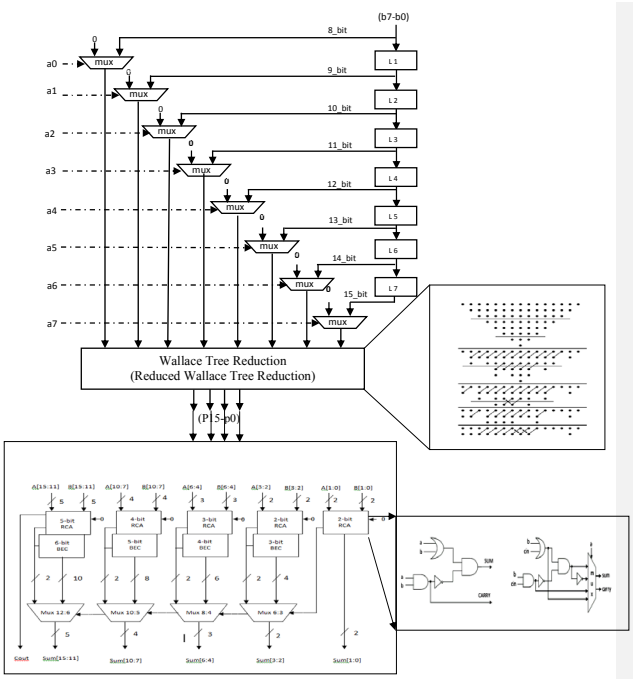

Figure 5. Structure of Modified Digital Russian Peasant Multiplier.

Figure 5 performs the multiplication operation functions based on RPM algorithm. As shown in Figure, 'n' multiplexors are required to perform 'n' bit multiplication operation. Reduced Wallace Tree Reduction (RWTR) process is applied on PPG results. Finally, 16-bit MSQRTCSLA adder has been used to add two 'n' bit binary data.

When compared to traditional Russian Peasant Multiplier architecture (Gunasakaran, K., and Manikandan, M. 2014), Modified Russian Peasant Multiplier offers 29.41% reduction of Slices, 29.91% reduction in LUTs and 26.03% reduction in delay consumption. Hence, developed MRPM is suited to different types of signal processing operations such as FIR filter, frequency transformation (FFT/IFFT), Convolutions and Correlations.

5. Proposed Modified Russian Peasant Multiplier using MSQRTCSLA based FIR Filter

In proposed design, 8-tap Direct Form Finite Impulse Response (DF-FIR) filter has been designed with the help of Modified Digital Russian Peasant Multiplier using MSQRTCSLA accumulation structure. The architecture

of proposed MDRPM using MSQRTCSLA based 8-tap FIR filter has been illustrated in Figure 6.

As shown in Figure 6, 8-tap FIR filter uses 8 MAC units to find the permitting and blocking frequency path. Z^{-1} indicates the delay elements, X[n-k] indicates the delayed version of input samples, h[1, 2, 3, ...n] indicates filter coefficients and Y[n] indicates the output sample. The dotted line of Figure 6 indicates the incorporation of proposed MAC unit into direct form FIR filter.

6. Simulation Results

Simulation result of proposed MDRPM using MSQRTCSLA based 8-tap FIR filter has been validated by using ModelSim 6.3C tool. It is a verification tool under in Mentor Graphics. The simulation result of proposed MDRPM using MSQRTCSLA based 8-tap FIR filter has been illustrated in Figure 7. In Figure 7, input sample X (n) is given as 50 in 8-bit binary data format. Different types of coefficient values are used based on different types of filter such as LPF, HPF and BPF. It takes 15 clock cycles for exhibiting the frequency paths.

7. Performance Evaluation

Proposed MDRPM using MSQRTCSLA based 8-tap FIR filter has been designed by using Verilog Hardware Description Language (Verilog HDL). To synthesize the proposed design, Xilinx 10.1i (Family: Spartan 3, Device: Xc3s50, Package: PQ208, Speed: -5) design tool

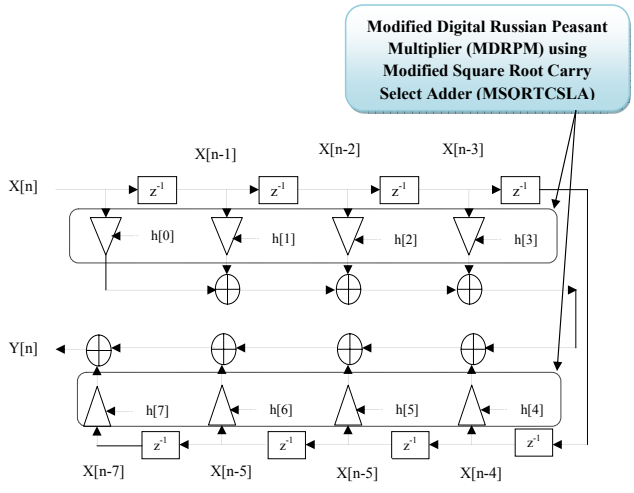

Figure 6. Architecture of proposed MDRPM using MSQRTCSLA based 8-tap FIR filter

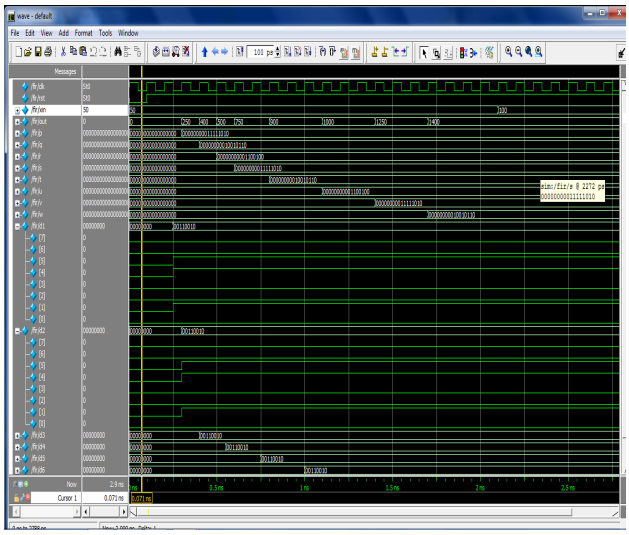

Figure 7. Simulation result of proposed MDRPM using MSQRTCSLA based 8-tap FIR filter.

Table 2. Synthesis Results of Existing RPM using BEC SQRTCSLA based 8-tap FIR filter and Proposed MDRPM using MSQRTCSLA based 8-tap FIR filter

Types/Parameters	Existing RPM using BEC SQRTCSLA based 8-tap FIR filter	Proposed MDRPM using MSQRTCSLA based 8-tap FIR filter
Number of Occupied Slices	171 (22% Usage)	93 (12%Usage)
Total Number of 4 input LUTs	281 (18% Usage)	150 (9% Usage)
Number of Slice Flip-flops	69 (4% Usage)	40 (2% Usage)
Minimum Period (ns)	8.744	6.788
Frequency (MHz)	114.364	147.325
Minimum Input Arrival Time Before Clock (ns)	1.662	1.636
Maximum Output Required Time after Clock (ns)	21.610	21.432
Quiescent Power (mW)	25	24
Dynamic Power (mW)	297	239
Total Power (mW)	322	263

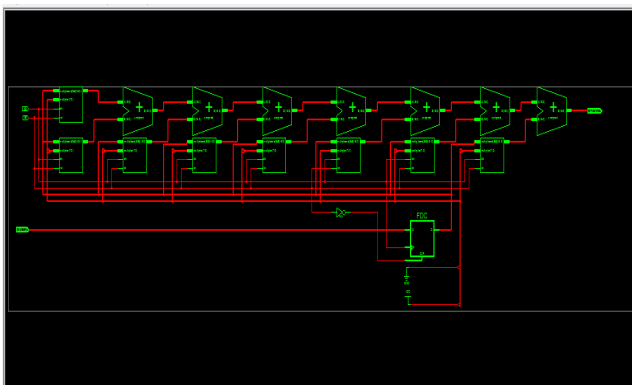

Figure 8. RTL View of Proposed MDRPM using MSQRTCSLA based FIR filter.

has been used. Synthesis results of existing RPM using BEC SQRTCSLA based 8-tap FIR filter and MDRPM using MSQRTCSLA based 8-tap FIR filter has shown in Table 2.

From Table 2, it is clear that Proposed MDRPM using MSQRTCSLA based 8-tap FIR filter offers 45.61% reduction in Slices, 46.61% reduction in 4-input LUTs, 42.02% reduction in Slice Flip-flops, 22.36% reduction in Minimum Period, 1.56% reduction in Minimum Input Arrival Time Before Clock, 0.823% reduction of Maximum Output Required Time after Clock, 19.52% reduction in Dynamic Power and 18.32% reduction in total power consumption than Existing RPM using BEC SQRTCSLA based 8-tap FIR filter. RTL (Register Transfer Level) View of Proposed DRPM using MSQRTCSLA based FIR filter has been illustrated in Figure 8.

8. Conclusion

In this paper, an efficient architecture for Finite Impulse Response (FIR) filter has been designed by using Modified Digital Russian Peasant Multiplier (MDRPM) and Modified Square Root Carry Select Adder (MSQRTCSLA). Verilog Hardware Description Language (Verilog HDL) has been used to design the proposed model. Traditional Multiplier architectures uses HAs and FAs based PPG generation and traditional adder structures like CSLA. But Gates using HA and FA should not help to improve the entire architectural performances. Hence, Russian Peasant Multiplier has been designed in this research work. Left and Right Shifters only used in RPM based Multiplication. Traditional structure of RPM has been modified in this paper by reducing one of the shifters, however it reduces the hardware complexity without alter any functionality. Modified SQRTCSLA accumulation structure has been used in the place of addition of MDRPM architecture. Proposed MDRPM using MSQRTCSLA based FIR filter offers 45% improvements in Area, 22.36% improvements in delay consumption and 18.32% improvements in power consumption than existing RPM using BEC SQRTCSLA based FIR filter.

9. References

1. Gunasakaran, K, Manikandan, M. Area efficient design of reconfigurable FIR filter using Russian peasant multiplier with modified carry select adder. International Journal of Innovative Research and Studies (IJIRS). 2014; 3(12):138–51.
2. Gunasakaran, K, Manikandan, M. High speed reconfigurable FIR filter using Russian peasant multiplier with Sklansky adder. Research Journal of Applied Sciences Engineering and Technology (RJASET). 2014 Dec; 8(24):2451–6.
3. Hatai I, Chakrabarti I, Banerjee S. An efficient constant multiplier architecture based on vertical-horizontal binary common sub-expression elimination algorithm for reconfigurable FIR filter synthesis. IEEE Transactions on Circuits and Systems-I. 2015 Apr; 62(4):1071–80.
4. Mohanty BK, Meher PK. A high-performance FIR filter architecture for fixed and reconfigurable applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems. 2015 Apr; 24(2):444–52.
5. Mohanty BK, Patel SK. Area–delay–power efficient carry-select adder. IEEE Transactions on Circuits and Systems-II. Express Briefs. 2014 Jun; 61(6):418–22.
6. Ramesh P, Beulet PAS. Design and implementation of low-power, area efficient FIR filter using different distributed arithmetic techniques. Indian Journal of Science and Technology. 2015 Sep; 8(21):1–5. DOI: 10.17485/ijst/2015/v8i21/79128.
7. Ramkumar, B, Kittur HM. Low-power and area-efficient carry select adder. IEEE Transactions on Very Large Scale Integration (VLSI) Systems. 2012 Feb; 20(2):371–5.
8. Ramu SS, Umadevi S. Realization of low power FIR digital filter using modified da-based architecture. Indian Journal of Science and Technology. 2015 Aug; 8(19).
9. Tyagi A. A reduced-area scheme for carry-select adders. IEEE Transactions on Computers. 1993; 42(10):1163–70. DOI: 10.17485/ijst/2015/v8i19/77161.
10. Waters RS, Swartzlander EE. A reduced complexity wallace multiplier reduction. IEEE Transactions on Computers. 2010 Aug; 59(8):1134–7.