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Design, Analysis and Simulation of memristor Emulator based Anti-aliasing filter for Biomedical Applications

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Abstract

Background/Objectives: This paper presents timing storage circuit based on memristor emulator. The memristor emulator includes most of the characteristics of real memristor. **Methods/Statistical analysis:** The considerable properties that a memristor embrace are wide range of memristance, bimodal operability of pulse and continuous input signals, long period of volatility, operability with other devices. The proposed timing storage circuit stores and reproduces timing information in analog manner without performing quantization. **Findings:** In design of continuous-time digital FIR filter, the analog delay blocks, which are implemented using memristor, are replaced with memristor emulator based timing storage circuit. **Application/Improvements:** It extends its benefits of storing and reproducing the CT digital signals, wide range of memristance, and anti aliasing processing. A CT FIR filter has been designed with memristor emulator based delay block as an example

Keywords: Biomedical Signal Processing, Continuous-time Digital Signal Processing, Memristance, Memristor Emulator, Timing Storage

1. Introduction

The basic conventional DSP system samples the input and the amplitude value is quantized at the discrete sampling time for the finite-bit representation. The two processes involved are: quantization of amplitude and discretization of time. CONTINUOUS -TIME (CT) Digital Signal Processor (DSP) operates in continuous time and discrete amplitude. It convenient many applications by combining thecharacteristics of both Analog and Digital signals. To get motivated for CT DSP is: the major difference between theContinuous DSP system and the conventional DSP system is that, in Continuous time DSP system, the happening of event in various instants are predicted while in conventional DSP system, the small signal may change for sampling instants, so the exact timing information is lost. The CT DSP system has much less in-band distortion and higher SDR.

Our body constantly communicates the information about our health[1]. Physiologic instruments are used to know that information that measures the heart rate, blood pressure, oxygen saturation levels etc.

The above measurements are analyzed and processed using biomedical signal processing to provide information usefulfor therapistto make conclusions. In recent days, engineers discover new methods to analyze and process these signals[2]. The biomedical signal like Electro Cardio Graphic (ECG) signals, the signal changes fast only in short instants where at many of the times the signal vary gradually with long delays. By processing such infrequently varying signals using conventional DSP, more power is wasted on many samples that carry

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redundant information[3]. By considering the adaptive power consumption of CT-DSP system, thismake more suitable for biomedical application.

The memristor is known as the fourth fundamental circuit element, thememristance value is as same as resistor byimparting the relation between voltage and current, but only at the fixed operating points.

The total charge passing through the memristor depends on the memristance of a memristor[4]. The considerable properties that a emulator circuit should constitute are the following, a wide range of memristance, bimodal operability of continuous and pulse signal inputs, a sustainedduration of non-volatility, floating operation, operability with other devices, and the ability for off-the-shelf devices implementation .The implementation of infinite Impulse Response (IIR) filter in CT-DSP system has many limitations thereby the Finite Impulse Response (FIR) filter with long tap delay makes a choice for its implementation[5]. As the biomedical signals varies infrequently the implementation of delay block in FIR filter becomes difficult.

As the biomedical signals has tapered bandwidth (few hundred Hertz) and the tap delay required for FIR filter is at the range of milliseconds. This makes the delay block implementation in FIR filter and also storing of CT digital signals to be difficult. The above limitations could be solved by memristor emulator based FIR filter, as it is more suitable for processing the low frequency biomedical signals. The design considerations for Continuous Time-Digital Signal processing system, CT-FIR filter and memristor emulator are described.

The infrequent varying timing information could be stored and reproduced using memristor emulator in an analog form by not quantizing the amplitude of timing information[6]. Thereby amemristor emulator with charge and memristance dependent characteristic based timing storage circuit is designed. Also, based on that CT FIR filter is designed for the anti-aliasing processing of biomedical signals. The designed CT FIR filter works at 3.3 Volts DC power supply with adaptive power consumption.

Analysis and design of memristor emulator with ability of wide range of memristance is introduced, in section 2. Using that memristor emulator based timing storage circuit is designed in section 3. Also, based on that CT FIR filter is designed using memristor is discussed in section 3. Section 4 includes observations and Section 5 features the conclusion.

2. Memristor Emulator

The circuits used in design of FIR filter are designed at a 0.35- CMOS technology with power supply 3.3-DC V. All the blocks are customized due to the absence of clock synchronization.

2.1 Memristor Emulator-based Timing Storage Circuit and Design of Memristor Emulator with A Wide Range of Memristance Variation

The considerable properties that the proposed memristor emulator should support are awide range of memristance, bimodal operability of pulse and continuous signal inputs and non-volatility. The proposed memristor emulator circuit includes all these features. The conventional memristor emulators have limitations particularly, the small variation in memristance and the non-floating operation are improved significantly. The memristance for an emulator is analyzed using mathematical expression. The proposed memristor emulator is a modified configuration having a small initial resistance R_s is shown in Figure 1.

At input terminal of Figure 1 the equation for voltage is

$$V_{in} = R_s i_{in} + \propto v_T v_C = (R_s + \propto R_T v_C) i_{in} \quad (1)$$

where, v_T is the voltage across the resistor, R_T, and $v_T v_C$ is the output of the analog multiplier. The sign of $\alpha R_T v_C$ is positive and not negative.

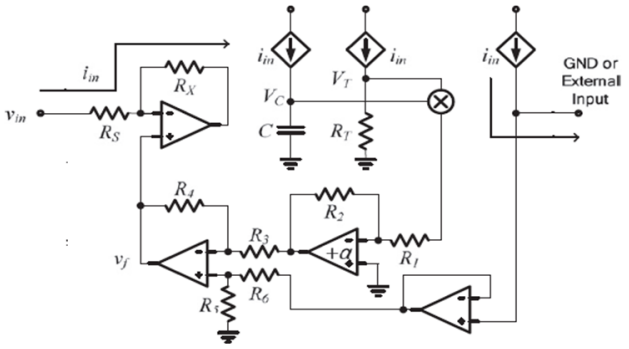

Figure 1. Block diagram for the memristor emulator circuit

Hence, the input memristance, R_{in}, is

$$R_{in} = R_s + \propto R_T v_C \quad (2)$$

Or

$$R_{in} = R_s + \frac{\propto R_T}{C} q(t) \quad (3)$$

It proves that from (3) that the input memristance is a linear function of charge q(t), thereby charge memristance dependent characteristic is achieved, although it is incremental.

Rearranging (1), we have

$$\propto R_T i_{in} v_C = v_{in} - R_s i_{in} \quad (4)$$

To maintain the equality in (4), the feedback voltage, $\alpha R_T i_{in} v_C$, should always belesser than v_{in}; namely,

$$\propto R_T i_{in} v_C < v_{in} \quad (5)$$

Hence, $\alpha R_T i_{in} v_C$, the output of the op-amp, is restricted not to reach the supply voltage V_{DD}. In other words, the saturation of op-amp will not clip its output, $\alpha R_T i_{in} v_C$. This is a major advantage over the existing memristor emulator since the input memristance is minimum due to the saturation of $\alpha R_T i_{in} v_C$. From (2), minimum input resistance is obtained, R_{in}, is R_S when v_C equals zero. For example, if we choose 100Ω for R_S, the memristance obtained will be equal to the minimum memristance of the HP memristor.

And also, the maximum memristance is computed as the ratio between the input voltage to the input current. As the voltage across R_s is v_{in}-$\alpha v_T v_C$, the current through R_s is

$$i_{in} = \frac{v_{in} - \propto v_T v_C}{R_s} \quad (6)$$

$$R_{in} \frac{v_{in}}{i_{in}} = \frac{v_{in}}{\left(v_{in} - \propto v_T v_C\right)} R_s \quad (7)$$

With (7), an infinitely large value of R_{in} can be obtained when $\alpha v_T v_C$ approaches v_{in}, as long as v_{in} is not zero.

An important result that could be pointed out is that $\alpha v_T v_C$ does not exceed V_{in} while the input memristance, R_{in}, varies from R_S to ∞. In addition, as the magnitude of the input voltage, v_{in}, should be less than the power voltage, V_{DD}, and the feedback value $\alpha v_T v_C$that is obtained without the saturation of any circuit components of the proposed memristor emulator configuration. The resultant input memristance range that can be obtained using the proposed circuit configuration is theoretically from R_S to infinity.

A prompt model of memristor emulator with charge memristance dependent characteristic and wide range of memristance is designed. The section follows with timing information storage concept

3. Timing Information Storage Cell

Memristor emulator can store and reproduce information as like memristor, thereby a timing storage cell is introduced based on emulator circuit. The basic idea is described in Figure 2.

At $t_1$instant, event X occurs; the memristor is connected in series with a constant current source, thereby the memristance will decrease[7]. At $t_2$instant, event Y occurs; the constant current source will be disconnected.

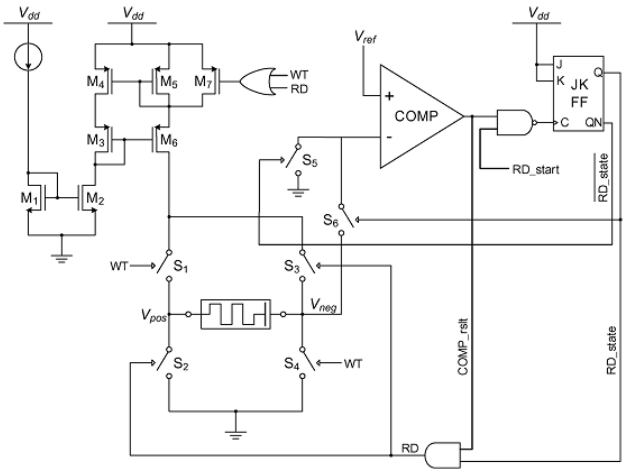

Figure 2. Schematic of a single timing storage cell.

The memristance value will stay constant at M_2. The difference between $M_1$the initial memristance and M_2 represents the time interval between events X and Y. The constant current source is reconnected to the memristor in opposite orientation for the reproduction of timing information.

3.1 Circuit Implementation

The schematic view of a single timing storage cell using single memristor is presented in Figure 2, the memristor is replaced with memristor emulator. The CT-FIR filter is designed using memristor emulator is shown in Figure 3.

Transistors M_1- M_6 forms a Wilson current mirror. Transistor M_7 forms switch. The J-K flip flop is configured to T flip flop by tying inputs J and K to V_{dd}. This triggers the starting and ending of the reproduction phase. First

the T flip flop has to be cleared, so that the "RD_state" and "$\overline{\text{RD\_state}}$" outputs will become "0" and "1" respectively. The comparator block is responsible for detecting the instance of V_{neg} crossing V_{ref}. By using delay block, the signal could be recorded and reproduced after τ delay. The delay block is implemented using four proposed memristor emulator based timing storage circuit. For efficient area and power utilization the current mirrors and comparators are to be shared between four cells.

The "RD_start" signals are generated using a 4- bit counter. This signal starts the reproducing phase in delay blocks. Once when the delay blocks start to reproduce, the generation of square wave by counter gets stopped. The CT digital signals storage could be achieved by using memristor emulator cells which provides wide range of memristance variation[8].

When the ADC block produces the "Change" pulse at its output, at the same timethe delay blocks are turns ON, to record the input. For the first "Change" pulse, "JK_DEL" signal is set only when the external square wave is "1" at the same time, and thereby enabling the counter. If "JK_DEL" is set and the external square wave is "0", then the counter AND DL1 and will be ON only after the arrival of next rising edge of the square wave[9]. The DL1 AND gate and DL2 AND gate are included here to assure that the counter will never get enable during setup or hold time of the internal flip-flops[10].

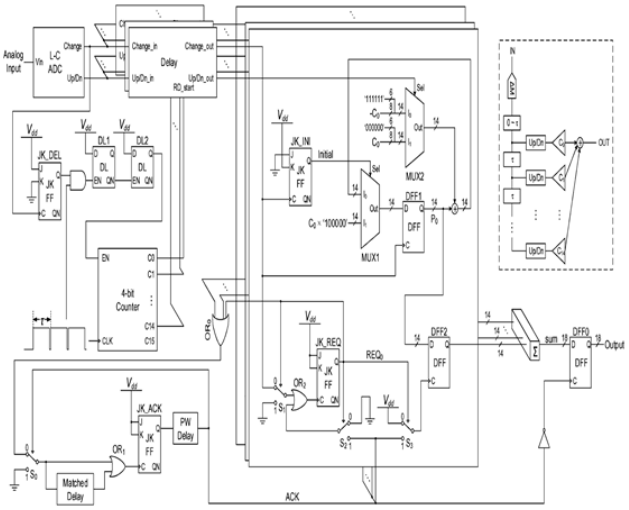

Figure 3. Schematic of a CT FIR filter.

At any instance, only one memristor cell can record and other is selected to reproduce the CT digital signal.

The ring counters are used to select the memristors cells in a circular order: after finishing recording or reproducing at the last memristor, from thefirst memristor, the operation gets continued[11]. The reusage of memristor cells, after each record/reproduce cycle, saves the total number of memristors cells needed. To assure the proper functioning, this condition has to be satisfied, that is, the memristor cells in the delay block should not be less than twice the number of samples that are produced in a period of $\tau_{n.}$. If this condition is not satisfied, the memristor may record an information that has not been reproduced yet[12], or the memristor may reproduce a timing information from the cell that has not completed its recording.

Multiplexed addressing techniques are employed for the memristor cell selection to be more efficient[13]. The current mirrors used for recording and reproducing could also be reduced to one, since, for signal to be stored, simultaneous recording and reproducing of information is needed not to be done simultaneously. The "Up/Dn" bit could be simplified to tap coefficient of FIR filter such that number of multipliers required could be reduced and power and area could be effectively utilized[14]. The leakage power consumed by memristor emulator in timing storage circuit is hardly negligible[15].

4. Observation

The simulation analysis is observed using Model sim. The output of Memristor emulator is expressed in Figures 4 and 5.

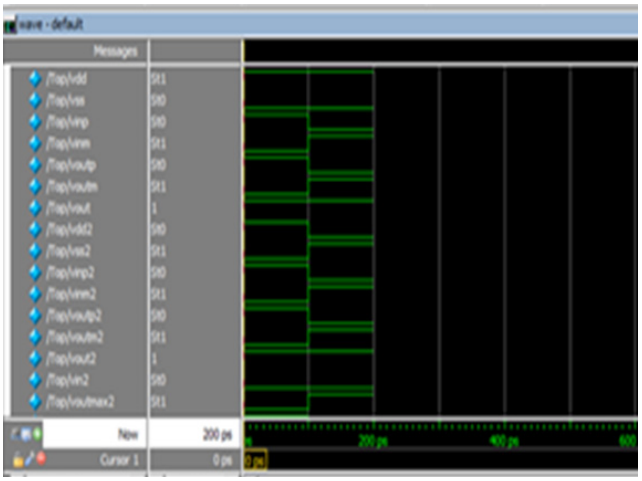

Figure 4. Output of Memristor emulator.

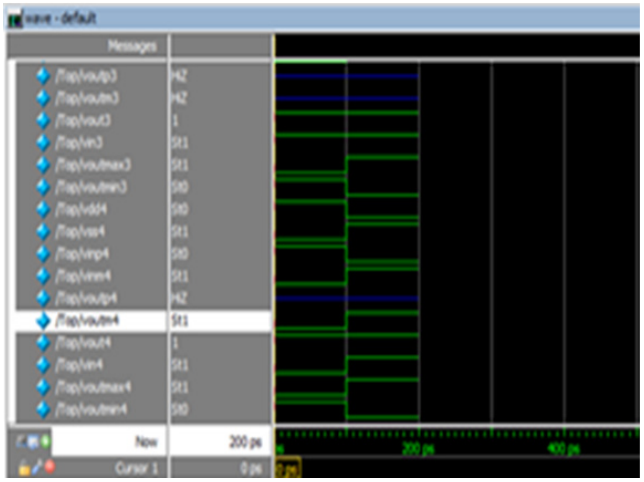

Figure 5. Output of memristor emulator.

The output for single cell timing storage cell using memristor emulator is shown in Figure 6.

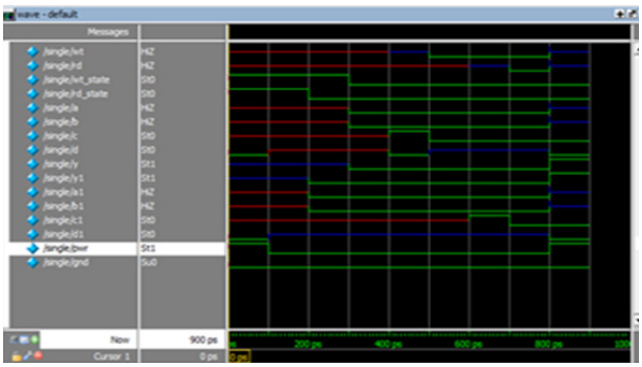

Figure 6. Output for single cell timing storage cell using memristor emulator.

The output for comparator in single cell timing storage cell using memristor emulator is shown in Figure 7.

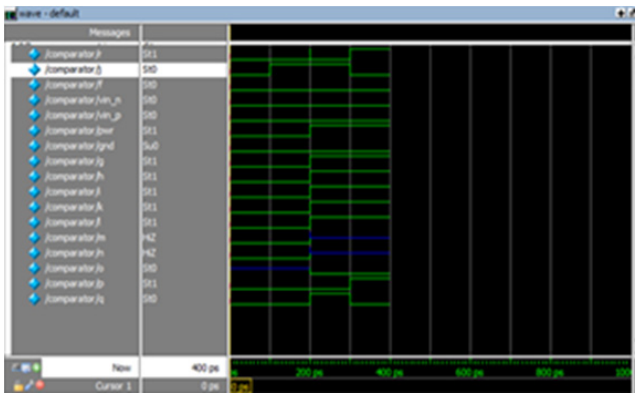

Figure 7. Output for comparatorsingle cell timing storage cell using memristor emulator.

The output for T flip flop in single cell timing storage cell using memristor emulator is shown in Figure 8.

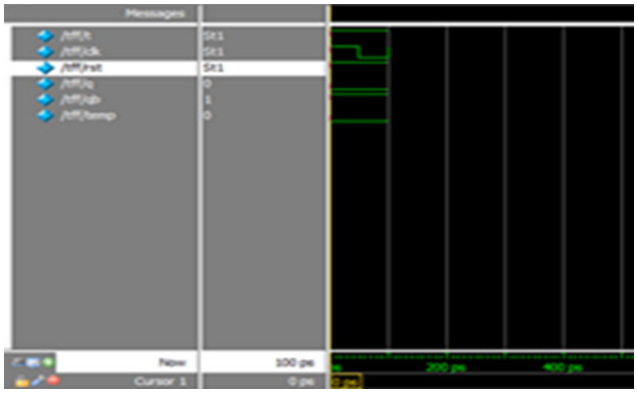

Figure 8. Output for T flip flop single cell timing storage cell using memristor emulator.

The output for counter in single cell timing storage cell using memristor emulator is shown in Figure 9.

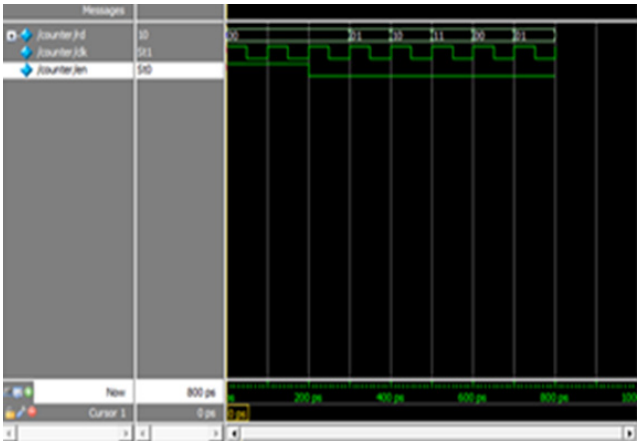

Figure 9. Output for counter in single cell timing storage cell using memristor emulator.

5. Conclusion

We have presented a new timing storage circuit based on memristor emulator. The emulator memristor circuit can also store and reproduce the timing information in analog form as memristor. When incorporated in a CT DSP system, this circuit allows the infrequent varying CT digital signals to be recorded and reproduced. A continuous time FIR filter is designed with memristor based delay block, which enables the effective utilization

of power and area. It extends its benefits of wide range of memristance, long period of volatility.

6. References

1. Praveena R, Nirmala S. Realization of efficient multiplier for low power biomedical signal processing system-on-chip design for portable ECG monitoring systems. Indian Journal of Science and Technology. 2015 Sep; 8(24):1–7. DOI: 10.17485/ijst/2015/v8i24/80211.
2. Hong Y, Lian Y, A Memristor. Based continuous time digital FIR filter for biomedical signal processing. IEEE Transactions on Circuits and Systems I: Regular Papers. 2015; 62(5):1392–401.
3. Yang C, Choi H, Park S, Sah MP, Kim H, Chua LO. A memristor emulator as a replacement of a real memristor. Semiconductor Science and Technology. 2015; 30(1):1–9.
4. Mahvash M, Parker AC. A memristor SPICE model for designing memristor circuits .53rd IEEE International Midwest Symposium on Circuits and Systems (MWSCAS). Seattle:WA; 2010. p. 989–92.
5. Chua LO. Memristor-the missing circuit element. IEEE Transactions on Circuit Theory. 1971 Sep; 18(5):507–19.
6. Pi S, Lin P, Jiang H, Li C. Device engineering and CMOS integration of nanoscale memristors. 2014 IEEE International Symposium on Circuits and Systems (ISCAS). Melbourne VIC; 2014. p. 425–27.
7. Li YW, Shepard KL, Tsividis YP. Continuous-time digital signal processors. IEEE 18th International Symposium on Asynchronous Circuits and Systems; 2005. p. 138–43.
8. Li Y W, Shepard K L, Tsividis YP. A continuous-time programmable digital FIR filter. IEEE Journal of Solid-State Circuits. 2005 Sep 18-21; 41(11):2512–20.
9. Schell B, Tsividis Y. A continuous-time ADC/DSP/DAC system with no clock and with activity-dependent power dissipation. IEEE Journal of Solid-State Circuits. 2008 Nov; 43(11):2472–81.
10. Hariprakash KP, Rajamani V. Modified architecture for hybrid passive optical networks, Proceedings of Recent Trends in VLSI Signal Processing, Communication and Embedded Technology. RVS College of Engineering and Technology, Dindigul: Tamilnadu; 2007.
11. Brückmann D, Feldengut T, Hosticka B, Kokozinski R. Optimization and implementation of continuous time DSP-systems by using granularity reduction, 2011 IEEE International Symposium on Circuits and Systems (ISCASE). Rio de Janerio; 2011. p. 410–13.
12. Burlingame E, Spencer R. An analog CMOS high-speed continuous-time FIR filter. University of California: USA; 2000. p. 1–4.
13. Weltin-Wu C, Tsividis Y. An event-driven clockless level-crossing ADC with signal-dependent adaptive resolution. IEEE Journal of Solid-State Circuits. 2013 Sep; 48(9):2180–90.
14. Arun C, Rajamani V, Selvi P, Muthukumaran S. Reduced Bit Error Rate (BER) VLSI architecture for convolutional decoder. National Conference on Recent Trends in Computer. Sri Venkateswara College of Engineering, Sriperumbudur: Chennai; 2006.
15. Arun C, Rajamani V, Revathi K, Anuradha S. Design and implementation of high rate pipelined architecture of Viterbi decoder. National Conference on Recent Trends in Computer Applications. Sri Venkateswara College of Engineering, Sriperumbudur: Chennai; 2006.