Indian Journal of Science and Technology, Vol 9(5), DOI: 10.17485/ijst/2016/v9i5/87170, February 2016
ISSN (Print) : 0974-6846
ISSN (Online) : 0974-5645

Implementation of HDB3 Encoder Chip Design

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Abstract

Background/Objectives: Digital communication is the process of transmission of the information which had been encoded digitally at the transmitter side and then passed through the channel encoder followed by the digital decoder at the receiver end. This paper majorly concentrated on low power synthesis and power analysis of HDB3 encoder. **Methods:** Alternative Mark Inversion (AMI) is a well-known data encoding technique for data encryption. HDB3 encoding is a derivative of AMI (Alternative Mark Inversion) encoding. The HDB3 code is one of the best representation codes which satisfies all the conditions of AMI and improves the limitations of AMI. **Findings:** The HDB3 encoder is designed with the help of V and B modules. It encodes consecutive zeros by inserting V and B in the form B00V. The VLSI architecture of the HDB3 encoder is implemented in Verilog HDL and the proposed design is synthesized and the results are compared with different TSMC technology libraries. The physical design of the chip is carried out in Cadence SoC Encounter tool. Low power synthesis results shows that the power required for the design is 17.65μW in 45nm technology. **Applications:** It has the ability to perform functions like Error correction/detection, provides better data encryption techniques in digital communication.

Keywords: AMI (Alternative Mark Inversion), Data Encryption, Encryption, HDB3, V and B Module

1. Introduction

The use of Digital Communication in present scenario has become very popular and worth[1,2]. Generally data transmission is not so simple, as it requires many necessary steps in order to provide user with uncorrupted output data. Problems like data missing, data damage, lack of synchronization was among the most common problems faced before digital communication was introduced. Digital communication helps to overcome such problems. It has the ability to perform functions like error correction/detection, provides better data encryption techniques. It is one among the most reliable data processing methods, easy to get data back at the output end and also allow data compression if the data is too large[3].

Data encoding is crucial in order to maintain the privacy of the data. The encoding techniques used depend upon the type of data and the information it contains. Generally there are many encoding techniques already in existence but they are not so efficient to provide correct data after decoding. The problem comes when input data contains continuous 0's. It may result is DC component if this type of pattern is encoded. So to avoid this problem a new encoding technique is proposed named HDB3 encoding technique[4].

HDB3 encoding technique is basically derivative of AMI encoding scheme[5]. The AMI encoding scheme makes sure that transitions or switching of the data are always present around each data bit. But, if long streams of zero's are present in the input sequence, there is possibility of data transmission uncertainty[6]. To overcome this, the encoder has to provide some switching in the data sequence or some violations. But those meant to be completely rectified at the receiver side. HDB3 encoding scheme is one the technique to increase the input data transitions so as to maintain efficient data transmission. It is widely used in all levels of European E-carrier system. HDB3 encoder is designed with the help of V and B modules. Its use is advantageous in the manner that the transmission code of HDB3 code has transmission efficiency and it encodes the consecutive 0's by inserting V (Violation Bit) and B (Insertion Bit) in the form like B00V, so as to overcome the problem of DC component.

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2. HDB3 Coding Methodology

The basic principle involved in HDB3 encoding is same as that in AMI (Alternate Mark Inversion) code. In AMI technique initially all 1's are represented with alternate sign polarity and all 0's are represented in same manner[7]. But here one may get consecutive sequence of 0's. The disadvantage of long stream of consecutive zeros is. The data may loss while transmission as well as, it may lose synchronisation with the receiver side.

So it is necessary to introduce some transitions in between long streams of zero and those transitions could be completely decoded at the receiver side. HDB3 encoder applies the concept of V and B insertion. One may consider this as data modulation technique. If the data contains the string of continuous 0's then the 4th bit of the string is replaced by the V, having polarity same as that of last non-zero bit. But still there remains the chance of getting DC component. Further for more precise and accurate result we used B (Inversion Bit) insertion. Here after V insertion, if in the data sequence one gets even number of 1's between two consecutive V, the 1st bit of the string is replaced by B having bit polarity opposite to that of last non-zero bit, else in all other conditions data remains the same[8, 9]. The flow chart of HDB3 encoder is shown in Figure 1. The symbols and binary values of HDB3 encoder are shown in Table 1.

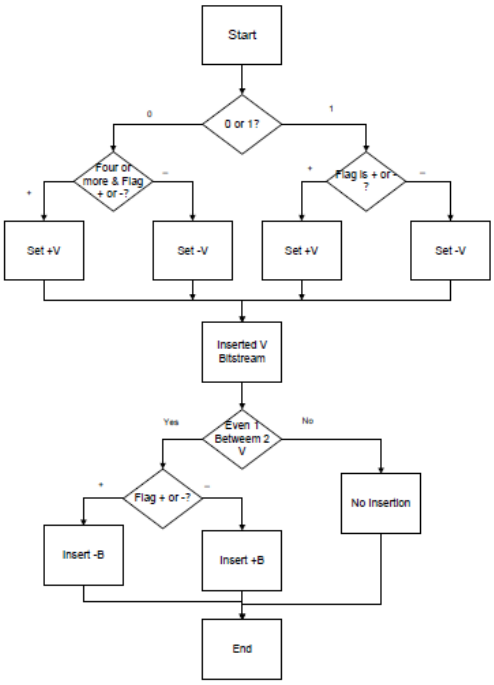

Figure 1. Flow chart for HDB3 encoder design.

2.1 Insertion of V Module

The conversion process of binary data starts with AMI encoding. The input to the decoder consists of long stream of zeros and ones. In AMI decoding technique, zeros are decoded and transmitted as zeros and ones are transformed as alternate +1 and –1. HDB3 encoding technique is derivative of AMI. Here, if the input sequence consists of continuous string of four or more than four zeros, it will replace the fourth zero with the violation bit V with the same polarity[10,11]. The polarity of this V depends upon the polarity of previous one, i.e. it takes the same polarity as that of previous one[12]. We have designed a counter to detect four consecutive zeros in the design. If it counts four or more than four zeros in the input data sequence, it automatically assign the fourth zero by violation bit V, with the polarity exactly opposite to the previous 1 in input data sequence[13]. Figure 2 shows the state diagram of insertion of V module.

Example: Consider the data stream:

1 0 0 1 0 1 1 0 1 0 1 1 0 0 0 0 1 1 0 0 0 0 1 0

It has 2 data streams which have 4 consecutive zeros. Hence 1 is replaced by alternating polarities (+1 and –1) and 0s are replaced as it is until data stream of four or more zeros has been detected. V is replaced with the last zero of four zeros with the sign associated with previous 1 detected:

+1 0 0 –1 0 +1 –1 0 +1 0 – 1 +1 0 0 0 +V –1 +1 0 0 0 +V –1 0

Table 1. Symbols and binary values of HDB3

Symbol	0	+V	+B	+1	–V	–B	–1
Binary	000	001	010	011	100	101	110

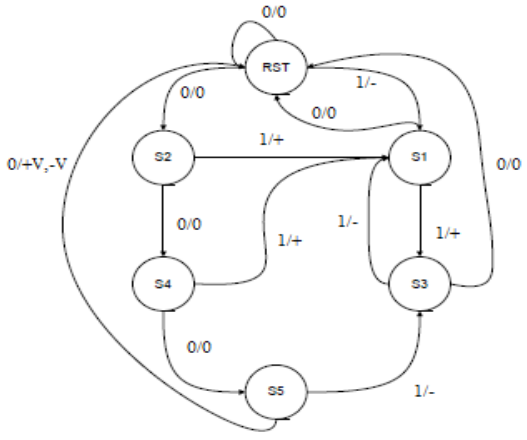

Figure 2. Insertion of V module.

2.2 Insertion of B Module

After insertion of V, the data stream goes through the upper level insertion i.e. insertion of inversion bit B[14–16]. This module checks the number of 1s (either +1 or –1) between two consecutive V (either +v or –V). If there are even number of 1s present in the data stream, then first zero of consecutive four zero bit stream is replaced by B, with the polarity opposite to that of previous 1. By the end of insertion of B module, the input bit stream is completely encoded. The insertion of B module is shown in Figure 3.

Example:
We have already V inserted data stream:

+1 0 0 –1 0 +1 –1 0 +1 0 –1 +1 0 0 0 +V –1 +1 0 0 0 +V –1 0

B is replaced with 1st zero of data stream which is exactly opposite of previous 1 detected:

+1 0 0 –1 0 +1 –1 0 +1 0 –1 +1 –B 0 0 +V –1 +1 –B 0 0 +V –1 0

3. Results and Discussions

The HDB3 encoder in designed using verilog Hardware Description Language (HDL) and the simulation results are shown in modelsim simulator. The simulation result of HDB3 encoder is shown in Figure 4. The design is verified with different test vectors and the results are extensively studied. The implemented design is synthesised using 45 nm, 90 nm and 180 nm TSMC libraries with the help of Cadence SoC Encounter. The physical design for the VLSI architecture is carried out using Cadence Encounter and shown in Figure 5. Power analysis and area analysis for the specified design is shown in Table 2 and Table 3 respectively. Low power can be achieved for the design with Low power Synthesis with a small area overhead. Using 180 nm technology library the power achieved for the design is 112 μW and by performing low power synthesis power reduces to 40.43 μW.

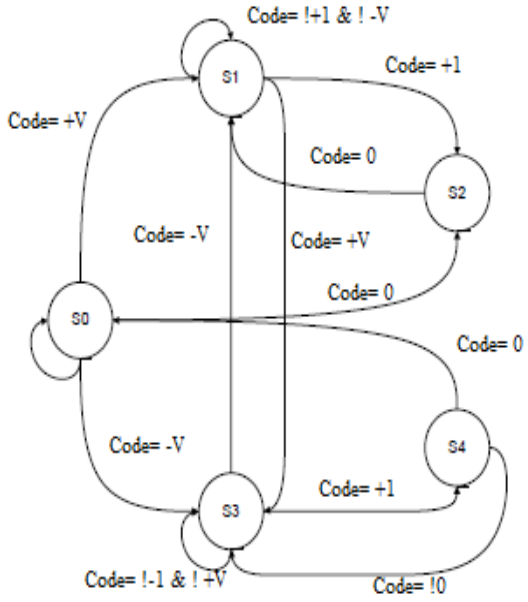

Figure 3. Insertion of B module.

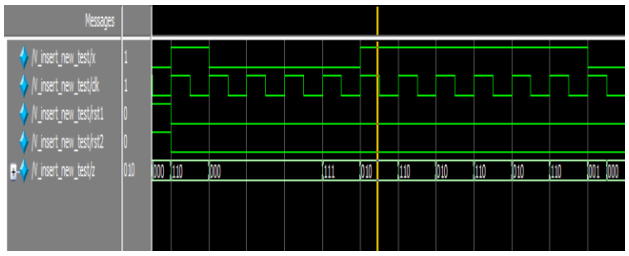

Figure 4. Simulation results.b

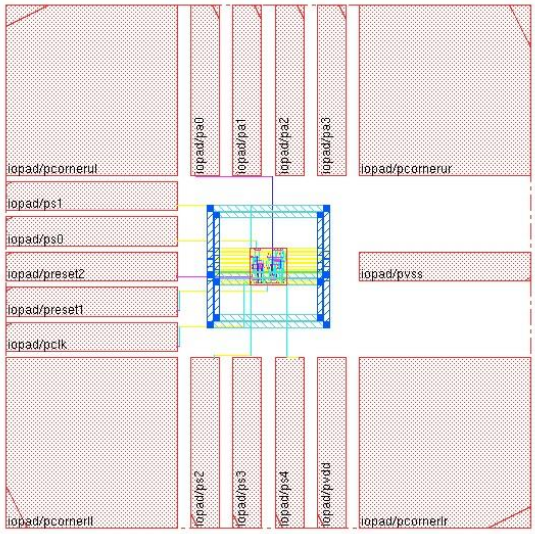

Figure 5. Chip layout.

Table 2. Power analysis

Technology Library	Logic Synthesis (μW)	Low Power Synthesis (μW)
45 nm	63.96	17.65
90 nm	89.23	37.78
180 nm	112	40.43
180 nm with DFT constraints	137.38	58.02

Table 3. Area analysis

Technology Library	Logic Synthesis (μm^2)	Low Power Synthesis (μm^2)
45 nm	201	239
90 nm	217	253
180 nm	236	280
180 nm with DFT constraints	243	297

4. Conclusion

This paper concentrated on a low power structure of HDB3 encoder design and it provides a better performance in digital communication applications. Therefore the ASIC implementation will reduce the number of external components required for data transmission. The power analysis results show that low power synthesis will even reduce the power required.

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