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Design and Performance Analysis of RAM_WR_ Control Module using Xilinx ISE 14.2

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Abstract

In the following work RAM_Write_Control module has been designed and its performance has been analyzed in terms of utilization of power and energy in order to make it energy and power efficient. The main idea behind this unit is to control the data write operation to the core which is used for saving the raw data in impedance measurement module of Electrical Impedance Tomography (EIT) system, KHU Mark 2.5. The performance of the unit is analyzed using 14.2 version of Xilinx software at Virtex-5 FPGA chip. The total power consumption of 3 logic families HSTL (High Speed Transceiver Logic), LVCMOS (Low Voltage Metal Oxide Semiconductor) and LVTTL (Low Voltage Transistor-Transistor Logic) at different I/O Standards have been compared in order to excrete out the most energy efficient logic family. Frequency scaling technique has also been applied by varying the frequencies at a scale of 100 Hz i.e., from 400MHz to 500 MHz to 600 MHz to 700 MHz in a way to find out the most power efficient frequency. It has been observed minimum power consumption occurs in case if we use LVCOMS15 I/O standard of LVCMOS logic family in comparison to other IO standards of other 2 logic families. And this maximum power savage occurs at a lowest frequency of 400 MHz.

Keywords: Energy Efficiency, EIT RAM, FPGA, System, WRITE CONTROL, Xilinx

1. Introduction

RAM stands for random access memory, which is used for the storage of data[1]. RAM_WR_Control is used to write the data to the RAM core and RAM_RD_Control is the module used to read data from the RAM Core. Just like in any FPGA based embedded system RAM forms a very important part of EIT systems. As shown in Figure 1, the RAM Core used in KHU Mark 2.5 EIT system is configured to be written first then read. The process of writing of RAM isstarted when it gets a command and information to be saved from the Data_Acquisition_Unit.

The RAM Core used in EIT system has RAM_WR_ Control module designed in Virtex-5 FPGA of XILINX[2] ISE 14.2 platform at 65nm technology. In Figure 2, schematic view of RAM_WR_Control is presented.

Figure 1. Working of RAMCORE module.

The Data_Acquisition_Unitsends the 16 bit data to the RAM_WR_Control module along with control signals. 16 Bit data line, 10 bit address line and RAM_ WR_En signal is generated in the RAM_WR_Control

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module. RAM_WREN is the pin which enables the data to be saved into the RAM Core.

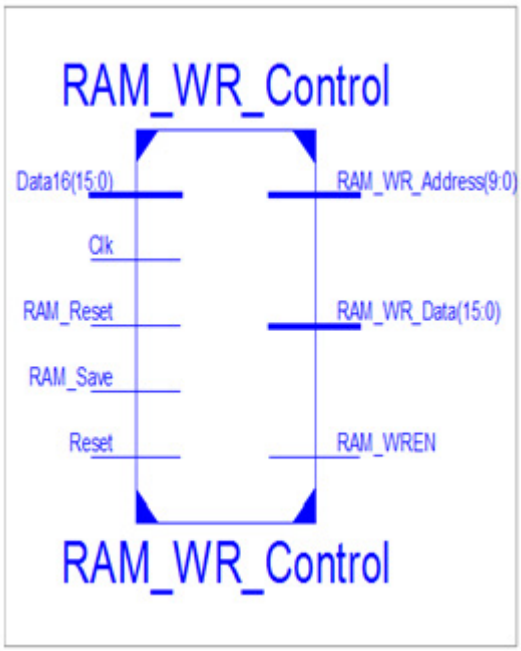

Figure 2. Schematic view of RAM writes control.

2. Related Work

RAM[1] is very important module for any processor to work. Much advancement has been done till date to improve its working so that it can work efficiently. UART (Universal Asynchronous Receiver/Transmitter) used to send data in serial is designed using Virtex-5 FPGA for different I/O Standards like LVTTL, HSTL_I,II, and III at XILINX platform. The same module was implemented on QUARTUS-II software from Altera also. The comparison is made of the two different tools' implementation and the best platform in terms of power efficiency is proposed[3]. The element for storage used in their work has one read port and one write port, having each port with separate address and data bus for reading and writing data[4]. They developed a modulator for tracking amplifiers in which they used CMOS technology. The results show 9% efficiency improvement when compared with previous architectures[5]. There is 90.2% reduction of input/output power when they used GTL I/O standard instead of GTLP_DC. Four different input output members of both GTL/GTLP_DC are being used[1]. Their main focus is to design efficient RAM for finite state machine. They checked the performance in terms of speed and area[6].

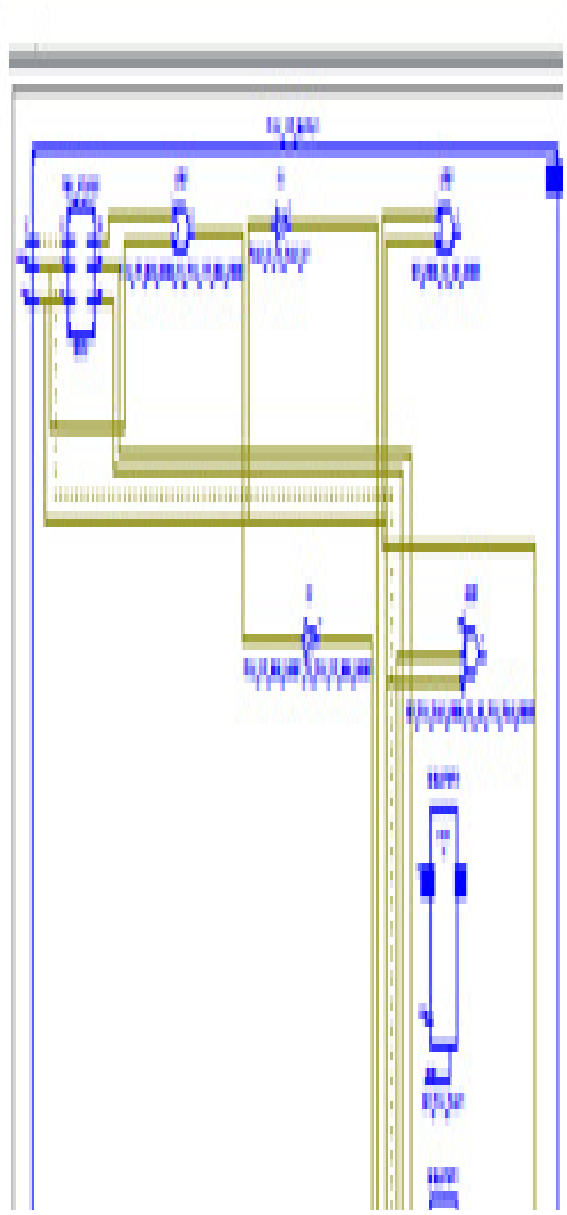

Figure 3. RTL view of RAM_Write_Control.

FPGA is being used to increase the performance and speed of the controller. They worked on multi-port controller so that memory can be directly accessed without processor's interference. With the help of this communication data can be transferred easily[7]. A 32 bit RSIC having each register of 32-bit is designed. The processor implements the four stage pipeline which is divided into Fetch, Decode, Execute and Write back. They have used Spartan 3E FPGA on XILINX ISE 14.7[8]. The authors implemented and designed a face detection technique using VIRTEX-5 LX330 field programmable gate array at operating frequency of 125.5 MHz. This technique is

used to detect faces at different scales[9]. A data processing device has been designed to make efficient data centre by applying different I/O standards operating on frequencies of 1.9 GHz, 2.4 GHz, 2.8 GHz and 3.4 GHz. This analysis is done on Intel and AMD processors and the energy efficient processor has been proposed[10].

3. Results

Figure 4. Different frequencies used for the analysis.

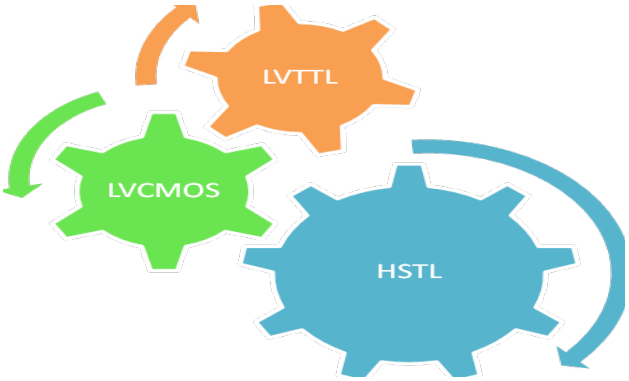

Figure 5. Different I/O standards used for the power analysis.

At operating frequency of 400MHz, there is 57.3% power curtailment when LVCMOS15 is compared with HSTL_I, II, III, IV and LVTTL. All these results are shown in the Figure 6.

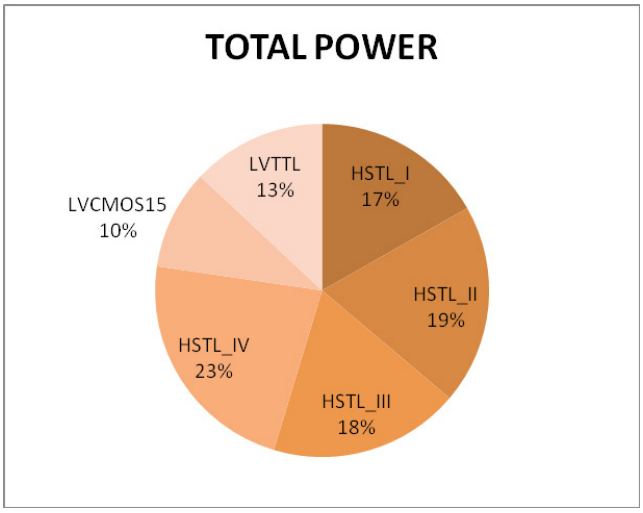

Figure 6. Power dissipation at various I/O standards as a percentage of total power (sum of power dissipation at various I/O standards) in XILINX at 400 MHz.

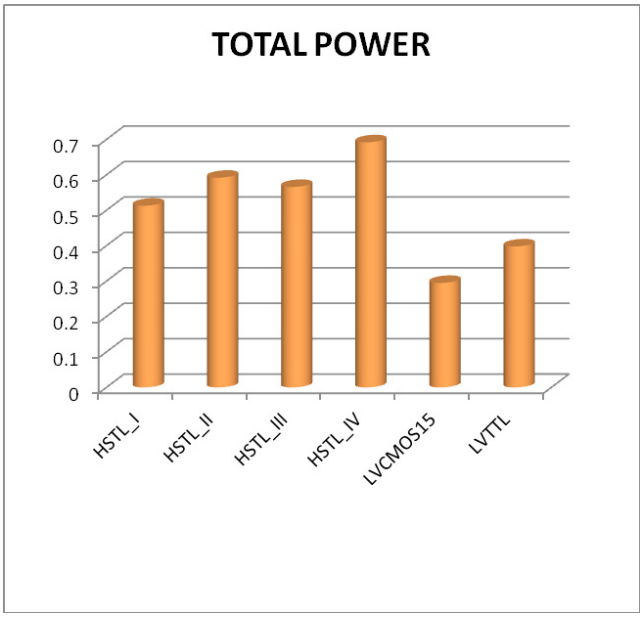

Figure 7. Power comparison of different standards at 400 MHz.

Table 1. Power dissipation at various I/O standards of RAM_WR_Control at 400 MHz

Standards	LVTTL	HSTL_I	HSTL_II	HSTL_III	HSTL_1V	LVCMOS15
Power(W)	0.398	0.513	0.592	0.566	0.692	0.295

Table 2. Power dissipation at various I/O standards of RAM_WR_Control at 500 MHz

Standards	LVTTL	HSTL_I	HSTL_II	HSTL_III	HSTL_IV	LVCMOS15
Power (W)	0.436	0.0519	0.596	0.575	0.700	0.308

When we worked using frequency of 500 MHz, we found out that there is curtailment of 56% power when LVCMOS 15 is compared with HSTL_IV. The above mentioned I/O standards are compared because they dissipate less and more power respectively. This analysis is done when LVCMOS is compared with all the different I/O standards. This observation is given in Figure 8 below.

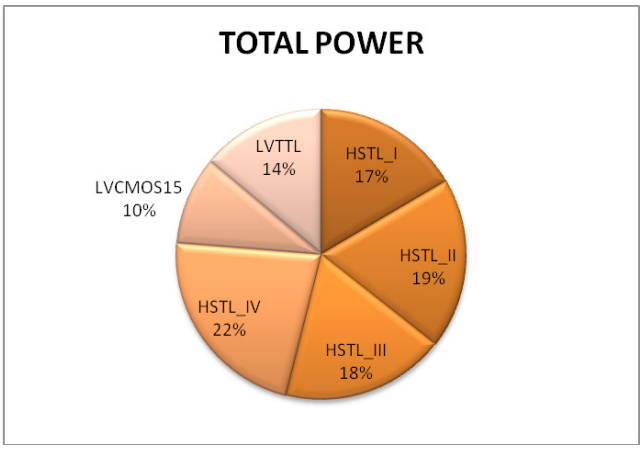

Figure 8. Power dissipation at various I/O standards as a percentage of total power (sum of power dissipation at various I/O standards) in XILINX at 500MHz.

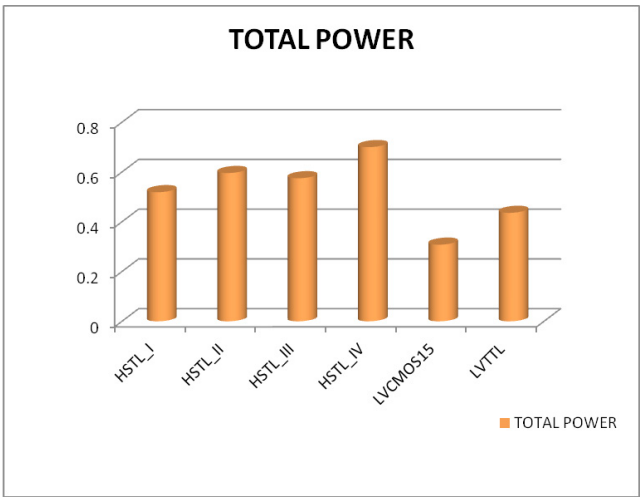

Figure 9. Power comparison of different standards at 500 MHz.

There is 54.87% dissipation of power at 600 MHz operating frequency. In this analysis also low voltage metal oxide semiconductor generates best results among all the standards as given in Figure 10.

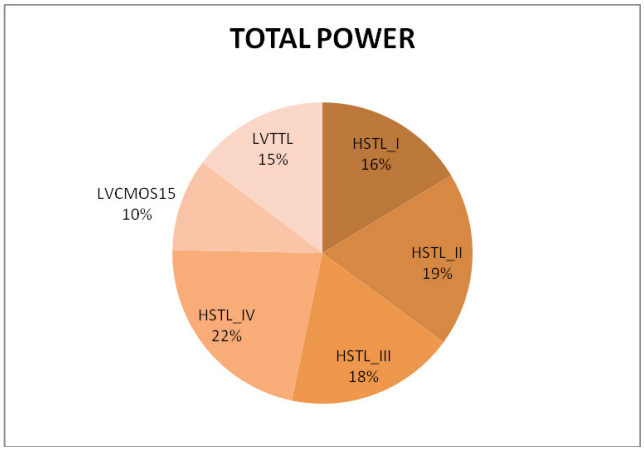

Figure 10. Power dissipation at various I/O standards as a percentage of total power (sum of power dissipation at various I/O standards) in XILINX at 600 MHz.

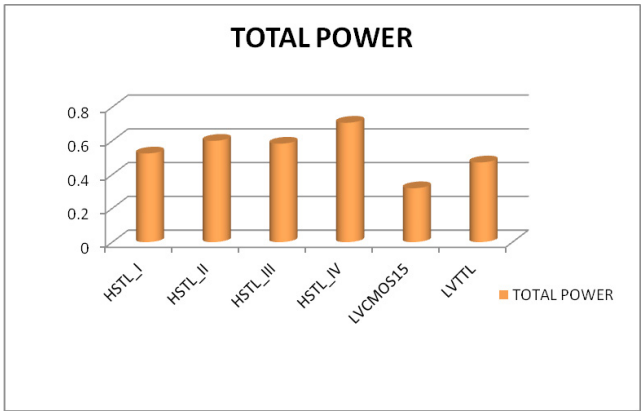

Figure 11. Power comparison of different standards at 600 MHz.

Power loss of 53.4% happens when the minimum power consuming LVCMOS15 is compared with the maximum power consuming HSTL_IV. This observation is presented in the Figure 12 shown below.

Table 3. Power dissipation at various I/O standards of RAM_WR_Control at 600 MHz

Standards	LVTTL	HSTL_I	HSTL_II	HSTL_III	HSTL_IV	LVCMOS15
Power(W)	0.525	0.6	0.583	0.707	0.472	0.319

Table 4. Power dissipation at various I/O standards of RAM_WR_Control at 700 MHz

Standards	LVTTL	HSTL_I	HSTL_II	HSTL_III	HSTL_IV	LVCMOS15
Power(W)	0.51	0.53	0.63	0.591	0.713	0.332

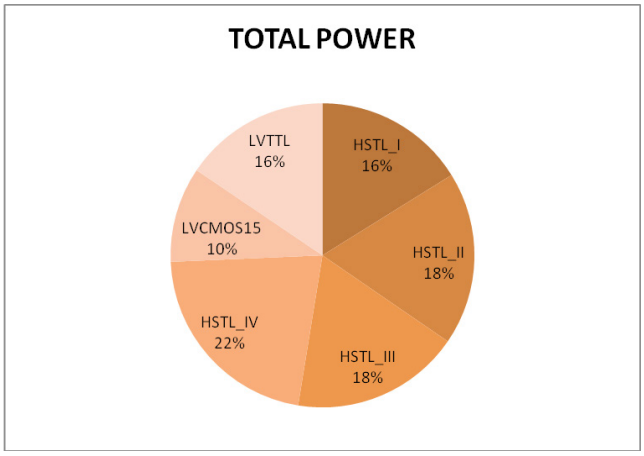

Figure 12. Power dissipation at various I/O standards as a percentage of total power (sum of power dissipation at various I/O standards) in XILINX at 700 MHz.

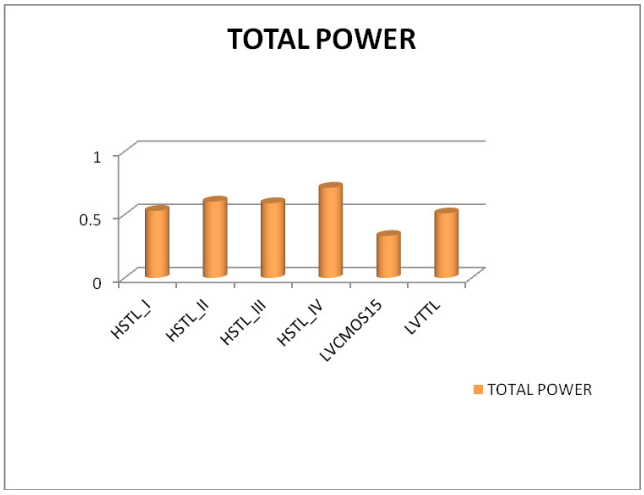

Figure 13. Power comparison of different standards at 700 MHz.

4. Conclusion

After analyzing, it has been observed that when we use LVCMOS15 apart from HSTL_I, HSTL_III, HSTL_IV, LVTTL there is a significant reduction of power. Different frequencies of 400MHz, 500 MHz, 660 MHz, 700 MHz has been used to find out the curtailment in the consumption of power by Ram WRITE CONTROL module. So, we can conclude that if we use LVCMOS15 at 400MHz, there is 53.4% reduction in power which is less in comparison to other frequencies mentioned above. By using low voltage metal oxide semiconductor at 400 MHz, we can make RAMWRITE CONTROL module energy efficient.

5. Future Scope

We have designed the RAM WRITE CONTROL module for EIT system and its analysis in terms of power has been done in XILINX platform. This analysis is done at 65 nm operating on 400 MHz, 500 MHz, 600 MHz, 700MHz frequencies. We will be extending our work by using different FPGAS and I/O standards for this module.

6. References

1. Moudgil A, Garg K, Pandey B, Hussain DA, Das B, Abdullah. GTL based Internet of things enable processor specific RAM design on 65nm FPGA. 57th IEEE International Symposium on ELMAR; 2015. p. 133–6.
2. Pandey B. Leakage power reduction with various IO standards and dynamic voltage scaling in vedic multiplier on Virtex-6 FPGA. Indian Journal of Science and Technology. 2016; 9(25).
3. Kaur H. Design and performance analysis of uart using Altera Quartus-II and Xilinx ISE 14.2. 6th International Conference on Communication and Network Technologies; 2016.
4. Sohal H, Wi H, Mc Ewan AL, Woo EJ, Oh TI. Electrical impedance imaging system using FPGAs for flexibility and interoperability. Biomedical Engineering Online. 2014; 3(1):126.
5. Salimi A, Atefeh S. A digital predistortion assisted hybrid supply modulator for envelope tracking power amplifiers. Integration, the VLSI Journal. 2016; 52:282–90.
6. Awate S. FPGA realization of multi-port memory controller for communication with DDR2 memory. International Journal of Emerging Research in Management and Technology. 2015; 4(6):244–6.
7. Navaro S. High-speed and area-efficient reconfigurable multiplexer bank for RAM-based finite state machine implementations. Journal of Circuits, Systems and Computers. 2015; 24(7):1550101.
8. Poduel A, Bikash P. Design and implementation of synthesizable 32-bit four stage pipelined RISC processor in FPGA using verilog/VHDL. Nepal Journal of Science and Technology. 2015; 15(1):81–8.
9. Jin B, Seunghun J. Design and implementation of a pipelined datapath for high-speed face detection using FPGA. IEEE Transactions on Industrial Informatics. 2012; 8(1):158–67.
10. Garg D, Kaur H. Processor specific data processing device for energy efficient data center. International Journal of Big Data Security Intelligence. 2014; 1:1-10.