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The BLIXER, Integrated Balun-LNA-Mixer for ZigBee Application

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Abstract

Objectives: The main objective of this paper is to design a Blixer using noise-cancelling technique and balun –LNA-Mixer for better performance. **Methods:** As studied in literature of mixers, it shows they have less bandwidth disadvantage. This paper is concentrated to realize a wide bandwidth mixer by keeping the real part of the impedance of all RF nodes low, and using this mixer there is no capacitive loading problem. **Findings:** By avoiding use of inductors, the on chip size of circuit will be reduced and also the bandwidth extension requirement is fulfilled. This gives less DC-voltage drop after IF filtering. The design is implemented and simulated using Advanced Design System tool in CMOS 0.18um technology. The noise figure of the final BLIXER is obtained as 0.6dB and that of LNA is less than 2dB. This results are one of the best seen for a BLIXER. **Applications:** This design is well suited for wideband ZigBee receiver in wireless communication systems.

Keywords: Balun, Blixer, LNA, Mixer, Wideband

1. Introduction

Design of low voltage, integrated CMOS based Balun, LNA and Mixer is challenging for low power transceiver applications. Wideband receivers are useful for Software Defined Radio (SDR) and Millimeter Wave Communication. Such applications, cover a wide frequency spectrum, which are also suitable for ultra wide band communication. Wideband radio receivers[1–3] has recently drawn significant research interest, e.g., for emerging SDR[2,3] architectures and Ultra-WideBand (UWB) communication standards.

Historically, Monolithic Microwave Integrated Circuits (MMICs) designed with III-V semiconductor technologies, have superior performance compared to CMOS. But, still a CMOS implementation promises higher levels of integration and reduced cost[1].

History of specifications targeting for WLAN and WPAN. The next generation 5G is a promising field for high speed and high data rate communication. For high data rate, wide bandwidth is necessary. IEEE 802.15.3-2003 for high data rate (>20Mbps). IEEE 802.15.3c 2009 employs Single carrier mode with PSK/QAM. No commercial equipment employs IEEE 802.15.3c. IEEE 802.11ad for wireless HD (High Definition). Wireless Gigabit Alliance completes wireless specification to set up wireless multimedia streaming. It supports data transmission rates up to 7 Gbps beyond 10m distance[1–4].

To connect the RF input to different RF filters and to the antenna networks. Recently, some wideband balun-LNAs[4–10] with high linearity have been proposed offering a wideband input match and gain. Active mixers have a capacitive input impedance, i.e., the gate of a transistor. When a passive mixer is used, a voltage buffer or transconductance stage is often required between the LNA output and the input of the mixer. Capacitive loading takes place with this intermediate stage.

Due to capacitance load, it is challenging to realize high LNA gain over a wide bandwidth. The proposed design of Blixer[7] topology is shown in Figure 1. The topology actually comprises an active Balun, LNA and mixer in a single circuit. Without bandwidth extension inductors. Impedance matching is done by transmission lines. Advanced Design System (ADS) is used for pre-

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layout and post layout simulation. Low Noise Amplifier is implemented in 180 nm Complementary Metal Oxide Semiconductor (CMOS) technology.

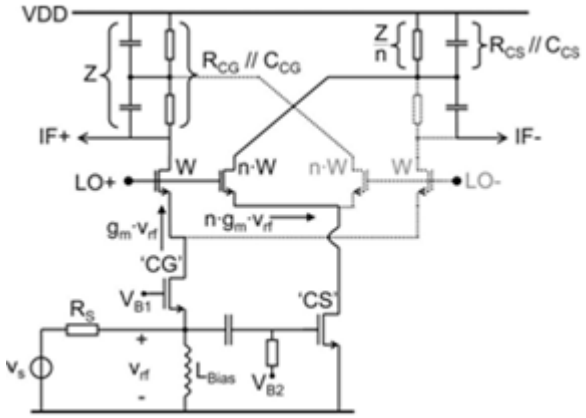

Figure 1. Proposed BLIXER topology.

2. Design Considerations

The key parameter of high frequency RF circuits are the conversion gain. The conversion gain of mixer is related to the trans-conductance stage and is given by

$$Av_{CG} = g_{mCG}.R_{CG}$$

where, Av_{CG} = gain of CG Amplifier

R_{CG} = Drain resistance of CG stage

where, g_m is given below

$$g_{m=}\frac{2I_D}{V_{GS}-V_{TH}}$$

$$g_{m=}\mu_n C_{ox}\left(\frac{W}{L}\right)\left(V_{GS}-V_{TH}\right)$$

Substituting g_m equation in gain equation

$$Av_{CG} = g_{m=}\mu_n C_{ox}\left(\frac{W}{L}\right)\left(V_{GS}-V_{TH}\right).R_{CG}$$

The loading capacitor C_L is

$$C_L < \frac{1}{2\pi .R_{CG}.F_{3dB}}$$

R_{CG} = Drain resistance of CG stage

Cascade capacitance c_{case}

$$c_{case} \approx c_{GDO} + C_{JB}$$

c_{case} = *cascadecapacitance*

c_{GDO} = gatedrain overlap capacitance

C_{JB} = drainbulk junction capacitance

Noise figure of amplifier

$$NF_{amp} = 1 + \frac{V_{n\ out}^{\ 2}}{a^2 A_v^{\ 2}}\frac{1}{V_{n\ RS}^{\ 2}}$$

$V_{n\ out}^{\ 2}$ = *amplifier noise at output*

$V_{n\ RS}^{\ 2}$ = *source impedance noise*

A_v = *The amplifier voltage gain*

The latest design using the popular 0.18umCMOS process. Table 1 gives the specification for the BLIXER design, carried out in this paper.

3. Balun LNA

Common Gate and Common Source circuits using NMOS transistor as active device is used in the design of LNA and Balun. These parallel stages are cascaded to enhance high voltage gain. A high voltage gain is achieved in the proposed design , through the resistors R_{CG} and R_{Cs} . The CG stage realizes wideband input impedance matching and gain, while the CS stage realizes an anti-phase output signal. Simultaneously noise canceling is done though CS and CG stages.

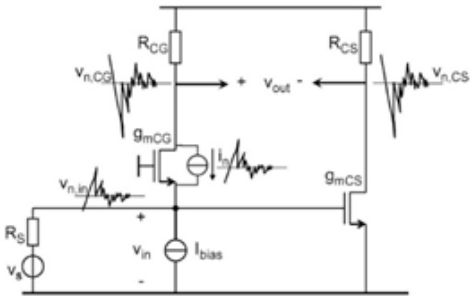

Figure 2. BALUN-LNA with CS and CG stages.

The Balanced to Unbalanced and Low noise Amplifier in Figure 2. It uses one CS stage and one CG stage. The voltage gain of CG stage can be measured by using

$$Av_{CG} = g_{mCG}.R_{CG}$$

As the gain of the Common Source stage is equal but with opposite sign

$$Av_{CG-cs} = 2.Av_{CG}$$

The total voltage gain of the CG-CS Low Noise Amplifier from single-ended input is two times higher than differential output.

The loading capacitance C_L is most critical at the Common Gate side

$$C_L < \frac{1}{2\pi.R_{CG}.f_{-3dB}}$$

The load capacitance is the sum of the input capacitance of the next stage (input stage of the mixer) and the capacitance of the cascode transistor.

$$C_{case} \approx C_{GDO} + C_{JDB}$$

Where the two dominant capacitances seen at the drain of the cascode are the gate-drain overlap capacitance C_{GDO} and the drain-bulk junction capacitance C_{JDB}

4. The Blixer Topology

The proposed design of BLIXER is shown in Figure 1, where the same CG and CS transistors are used. There are two types of mixers, current commutating and voltage commutating mixers. Current commutating is preferred in this design. As well as, Cascode configuration is preferred in order to increase the overall gain factor. Instead of one, both the CG and the CS side have now two Cascode (or mixer) transistors, while the cascode transistors are now part of a current commutating mixer. They are periodically switched on and off, with frequency f_{LO} .The current from the CG and CS transistor always flow towards the load , as at any moment in time one of its mixer (cascode) transistors is active .At the drains of the mixer ,down conversion to an Intermediate Frequency (IF) takes place, which is much lower than the RF frequency.

In the BLIXER topology, the capacitance at the loads sets the *IF bandwidth*, instead of the *RF bandwidth* in case of the balun-LNA. As the IF bandwidth is much lower than the RF bandwidth, the capacitance at the loads can be much higher. Furthermore, the capacitive load of the next stage can be absorbed into the capacitance of the IF filter. The bandwidth problem at the load of the CG stage, described in the previous section, is thus solved without inductors for bandwidth extension.

The voltage conversion gains from single-ended input to differential output of the BLIXER topology (Figure 2) can be calculated as

$$G_{BLIXER} = \frac{2}{\pi}.(g_{mCG}.R_{CG} + g_{mCS}.R_{CS})$$

The average voltage drop across the load resistors in the BLIXER is

$$\bar{V}_{LOAD} = \frac{1}{2}(I_{CG}.R_{CG} + I_{CS}R_{CS})$$

half of the period the CG transistor bias current I_{CG} flows throug hR_{CG} and in the other half the CS bias current I_{CS} a current flows through R_{CS}

$$S(t) = \cos(\omega_{signal}t).\cos(\omega_{LO}t)$$

$$= \frac{1}{2}\cos(\omega_{signal}t - \omega_{LO}t)$$

$$+ \frac{1}{2}\cos(\omega_{signal}t + \omega_{LO}t)$$

Were down converted signal used as IF signal and up converted signal is removed by IF filter.

Impedance is given as

$$Z = (R + SL) + (G \| \frac{1}{sc})$$

If L is zero and capacitance is infinite then it act as resistance.

(Figure 3) and (Figure 4) shows the schematic of Balun-LNA and BLIXER simulated in Advanced Design System.

Table 1. Specification of proposed design

PARAMETER	VALUE
NF	0.6dB
S_{11}	<-10dB

TECHNOLOGY	0.18µm
Gain	1.4dB
area	0.019 u sq m

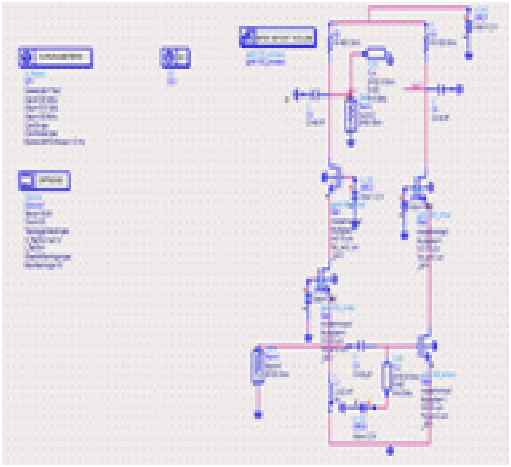

Figure 3. Schematic of Balun-LNA.

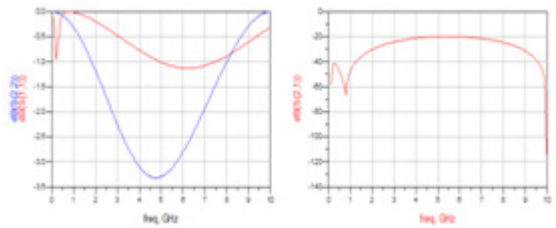

Figure 4. S parameters of Balun-LNA.

5. Simulation Results

The simulation results reveal that the proposed design, have a positive gain. Figures 5 and 6 give the

S-parameter results. S_{11} isless than 10dB. S_{21} is 1.4dB. The noise figure of the Balun-LNA and BLIXER is shown in Figures 7, 8. Figure 9 shows the value obtained for S_{11} , S_{12}, S_{21}, S_{22} .

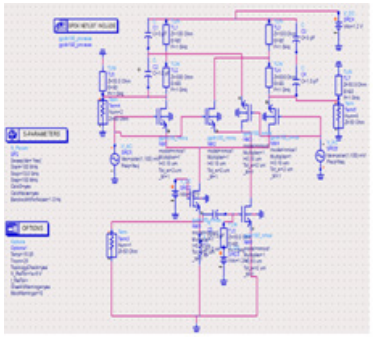

Figure 5. schematic of BLIXER topology.

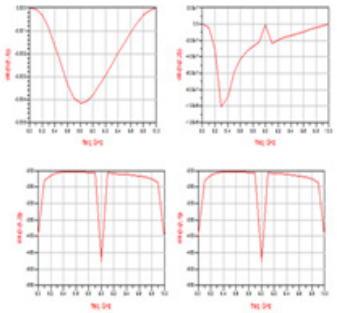

Figure 6. s-parameters of BLIXER.

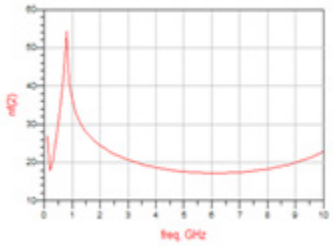

Figure 7. Noise figure of Balun-LNA.

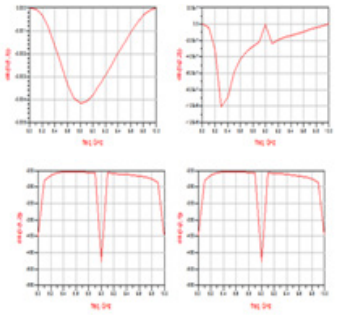

Figure 8. S parameters of blixer.

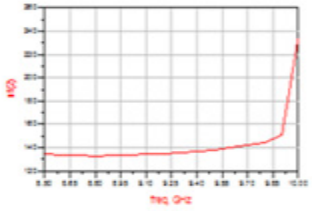

Figure 9. noise figure of BLIXER.

6. Conclusion

In this paper a BLIXER topology with noise cancelling balun LNA for wireless communication applications,which can be used for ZigBee communication is presented. By using this technology S_{11} is <-10dB

and noise figure is 11.5dB. The noise figure and conversion gain give best results ever reported before.

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