Indian Journal of Science and Technology, Vol 9(45), DOI: 10.17485/ijst/2016/v9i45/106366, December 2016
ISSN (Print) : 0974-6846
ISSN (Online) : 0974-5645

Real Time Computer Vision Systems for Rice Kernels

Bhupinder Verma[1*] and Gurpreet Kaur[2]

[1]PTU Kapurthala, Jalandhar - 144603, Punjab, India; verma_bk1@rediffmail.com
[2]CT Group of Institutions, Jalandhar - 144008, Punjab, India; gpreet.09@gmail.com

Abstract

Objectives: This paper presents a Morphological operations based software code in MATLAB for counting connected rice kernels from digital image and to grade the quality of samples by a methodology used by the Bureau of Indian standards. **Methods/Statistical Analysis:** The proposed code may further be transferred on to the reprogrammable hardware devices like FPGA by converting the entire code into VHDL (VHSIC Hardware Description Language) with the help of Simulink HDL Coder; making it a hardware compatible code. The efficiency of proposed code is tested over the digital images of rice grain samples with complex backgrounds or captured under poor illumination conditions. **Findings:** 100% accuracy has been observed in the counting efficiency of software and hardware codes by successfully separating touching kernels. The automatically generated VHDL code through HDL Coder is also successfully synthesized over the FPGA in Xilinx ISE and is compared for its accuracy and processing time with simulated results. It is concluded that a real time image processing algorithm, when design effectively to get synthesized over the FPGAs, may yield faster results with processing time of few seconds, whereas the manual methods or simulated methods are much slower in terms of their speed. **Application/ Improvements:** The proposed approach may further be utilized to design a portable FPGA based hardware prototype to grade the quality of rice samples by completing eliminating the manual investigation done by humans as well as by computer based simulated inspection.

Keywords: Embedded Imaging, FPGA, HDL Coder, Image Processing, MATLAB, VHDL, Xilinx ISE

1. Introduction

Food quality and safety is gaining paramount importance these days due to acting of food laws. Various countries have introduced food safety and quality management systems such as ISO 9000 and HACCP (Hazard Analysis Critical Control Point). US Department of Agriculture (USDA) continuously reviews strict use of standards for grading agricultural products for ever-expanding markets. In India, Government has established Food Safety and Standards Authority of India (FSSAI) under Food Safety and Standards Act, 2006 to bring out a single statutory body for regulating food laws and its enforcement. Moreover, recently reported food borne illness out-breaks have made consumers cautious towards better quality. To ensure better quality produce and compliance of the latest food laws, everyone in the trade need to re-evaluate quality to prevent any food borne diseases[1,2].

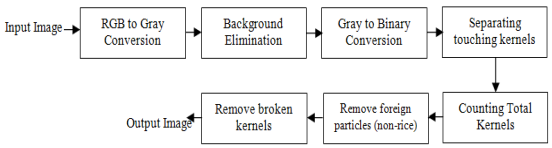


Figure 1. Process flow diagram for rice kernels.

Computer based automated systems have been reported in good numbers in the recent years. In[3] has identified two major factors which may hamper the speed of detection and grading of agro products using computer vision systems:

i. As compared to manufactured products, natural products are difficult to classify and grade and require much higher data processing speeds.

ii. The pace at which hardware equipment for material handling and separation is being developed is

*Author for correspondence

relatively slower as compared to computer hardware technology.

To achieve real-time results, many efforts have been reported to increase the speed of processing and to build real time computer vision systems[4–7]. This paper presents yet another effort using MATLAB Simulink HDL coder and mapping image processing algorithms on to hardware primarily Field Programmable Gated Arrays (FPGA).

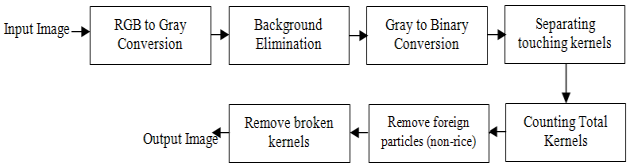


Figure 1. Process flow diagram for rice kernels.

2. Design Methodology

Real time computer vision systems need to acquire process and analyze image data to produce decision in numerical or symbolic form. Images of the rice kernels used in this research have been acquired using conventional color camera. The process followed for rice kernel classification in software code designed in MATLAB is demonstrated in a flowchart (Figure 1).

The code accepts all type of input images and converts the input image to *Grayscale* if it is RGB[8]. Further, the *background* is separated from the foreground in order to nullify the impact of complex backgrounds or poor illumination factors in the analysis of foreground. In subsequent stage, the Grayscale image is converted into *Binary* because the morphological operations[9] to be used for further analysis are binary dilation and erosion. The choice of these operations depends over their feasibility to get converted into VHDL code through HDL Coder.

It is pertinent to note that the binary erosion will decrease the size of objects in input image, therefore to *separate touching kernels*, the binary erosion is performed, but, it may also decrease the size of already thin rice kernels too much, therefore, successive dilation is performed with the size of SE less than that of the SE used for binary erosion. The rice kernels get successfully separated using this successive erosion and dilation technique. Further, total rice kernels are *counted* using morphological counting operation[9].

In order *to remove foreign particles,* i.e., the objects that are preferably not rice kernels or are discolored, the maximum (M) is found using morphological processing and all those connected pixels having size less than 1/8th of M are eliminated from the image[10].

Finally, the total kernels in the image are counted again that are having number of connected pixels greater than 50% and 60% of M. These are classified as medium and long kernels respectively.

The steps used in Simulink HDL Coder to automatically generate the VHDL code from the MATLAB code are also presented (Figure 2).

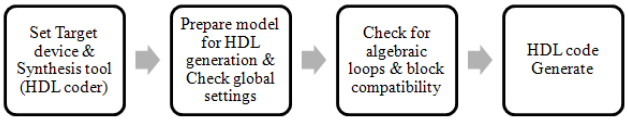
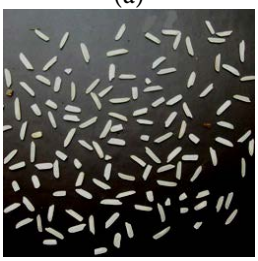


Figure 2. Steps for generating HDL in simulink HDL coder.

The proposed grading algorithm for the rice kernels has been successfully tested using MATLAB. Images of the rice kernel have been taken with a resolution of 256x256. Three types of input images are considered for the testing of the algorithm (Figure 3(a, b, c)). These images are first converted into binary [Figure 4(a, b, c)], thereafter the touching kernels are separated using successive erosion and dilation (Figure 5(a, b, c)). Finally the total numbers of grains are counted with & without separating broken and foreign kernels (Figure 6(a, b, c)) and (Figure 7(a, b, c)). Touching kernels are singulated and counted separately for the broken one and the wholesome using the image processing methods. The discolored (defective) grains are also not counted to enhance the grading.

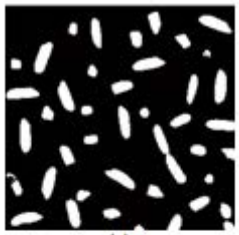
(a)



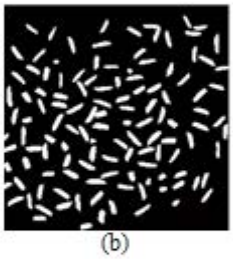
(b)

(c)

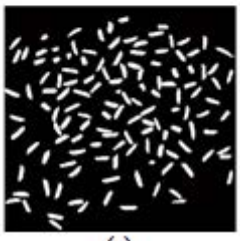
Figure 3. Original images of rice kernels.



(a)



(b)



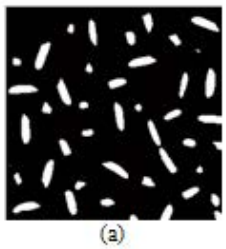
(c)

Figure 4. Results after binary operations.

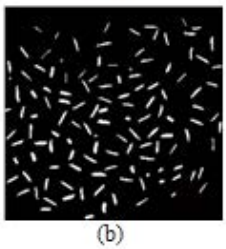
Thereafter the same image processing operations were mapped on to target hardware device FPGA through Simulink HDL code synthesis. The output images are obtained through Simulink HDL Coder for Binary Dilation (Figure 8(a)) and Binary Erosion (Figure 8(b)). Finally, the operation timings were noted for both simulations and synthesis.

3. Results and Discussion

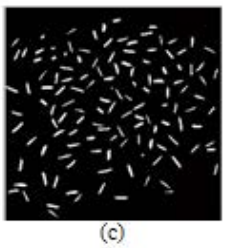
Counting results exhibit perfect counts for simulated results as well as hardware synthesis (Table 1). The results



(a)

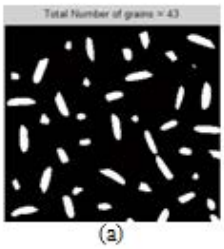


(b)



(c)

Figure 5. Results after separating touching kernels.

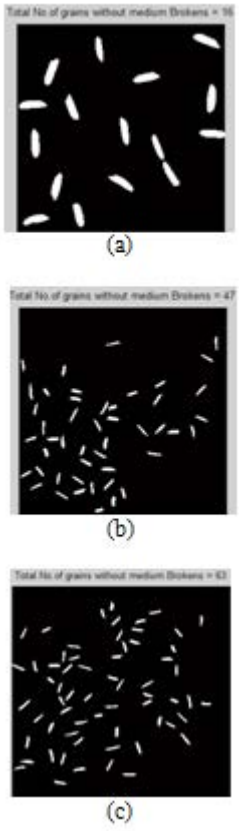


(a)

(b)

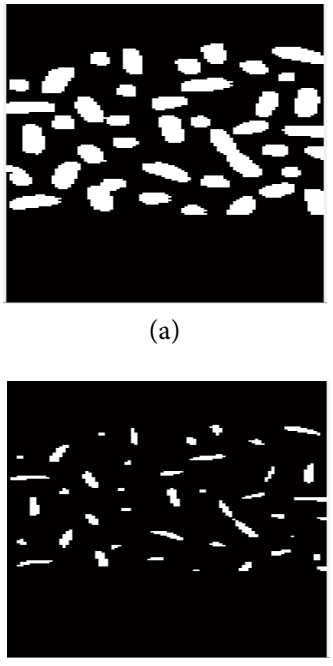
(c)

Figure 6. Counting total grains.



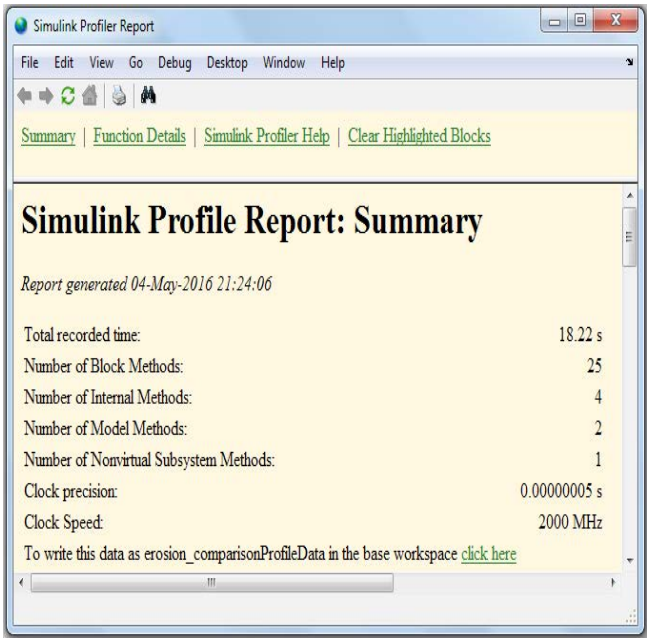
(a) (b) (c)

Figure 7. Counting medium kernels after eliminating foreign particles.



(a) (b)

Figure 8. Counting medium kernels after eliminating foreign particles.



(a)

```
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 5.360ns (frequency: 186.569MHz)
  Total number of paths / destination ports: 6994 / 208
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
  Total number of paths / destination ports: 349 / 349
--------------------------------------------------------------------------------
Offset:          3.710ns (Levels of Logic = 1)
  Source:        reset (PAD)
  Destination:     DelayIn_out1_0 (FF)
  Destination Clock: clk rising
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 1 / 1
--------------------------------------------------------------------------------
Offset:          3.819ns (Levels of Logic = 1)
  Source:        DelayOut_out1 (FF)
  Destination:     Morphedimg (PAD)
  Source Clock:    clk rising
iming constraint: Default path analysis
  Total number of paths / destination ports: 1 / 1
--------------------------------------------------------------------------------
Delay:           5.972ns (Levels of Logic = 2)
  Source:        clk_enable (PAD)
  Destination:     ce_out (PAD)

Total REAL time to Xst completion: 7.00 secs
Total CPU time to Xst completion: 7.39 secs
--------------------------------------------------------------------------------
```

(b)

Figure 9. Screenshots of processing time computation in. (a) Simulink. (b) Xilinx ISE.

are quite accurate. The grading of rice samples in three input images using the analytical formulas used in manual inspection of Indian standards is also computed (Table 2).

Finally, the processing time of simulated results of MATLAB (Simulink) are compared with that of synthesized results (Table 3). The screenshots of timing results

Table 1. Comparison of rice kernel counting

Comparison Factor	Input Image	Result of Manual analysis	Result of Simulated analysis	Result of Synthesized analysis	Accuracy
Total Number of Kernels	Image1	43	43	43	100%
	Image2	127	127	127	100%
	Image3	132	132	132	100%

(execution time) for simulation and synthesis are also presented here for comparison purpose (Figure 9).

Hence, the results indicate that an accurate and real time imaging system can be designed to grade the rice kernels.

Table 2. Grading of rice sample

Parameter	Image1	Image2	Image3
Total fine de-husked grains (N)	16	47	63
Total broken grains	27	80	69
Total grains by considering 3 broken as 1 whole grain (W)	25	74	86
Percentage of de-husked grains (N/W)*100	64	63.5	73.2

Table 3. Comparison of total processing time

Type of analysis	Tool used	Image size	Total processing Time (s)
Simulated	Simulink (MATLAB)	256×256	18.22
Synthesized	Xilinx ISE	256×256	7.39

4. Conclusion

This paper has tried to estimate speed of image processing operations used for classification and grading of agro-products particularly apples and rice grains. Operation timings obtained in processing time of FPGAs are of the order of ns i.e., 100,000 times or faster than simulators. The results indicate that the future computer vision systems may be much faster and real time, provided the other associated systems are also designed appropriately so that these do not become bottleneck.

5. Acknowledgements

The authors are grateful to Lovely Professional University, Phagwara, Punjab for facilitating this research.

6. References

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