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Low Power, High speed, Low leakage Floating Gate SRAM Cell using LECTOR Technique

Kanan Bala Ray[1], Sushanta K. Mandal[2] and B. Shivalal Patro[1*]

[1]KIIT University, Bhubaneswar - 751024, Odisha, India; kananray@yahoo.co.in, shivalalpatro@gmail.com
[2]Centurion University, Bhubaneswar - 752050, Odisha, India; sushantakumar@yahoo.com

Abstract

Objective: Leakage power is the major concern of circuit designers in nano meter technology era. The objective of this work is to design a low leakage power floating gate MOS static random access memory. **Methods/Statistical Analysis**: The proposed design has been made using Floating Gate MOS (FGMOS) and Leakage Control Transistor (LECTOR) technique. FGMOS has been used in place of normal MOS on the conventional SRAM cell. In the LECTOR an NMOS transistor is incorporated between output and pull down the network and a PMOS transitor is incorporated between output and pull up a network. **Findings:** The SRAM cell has been designed and simulated in Cadence environment on 45 nm gpdk standard CMOS process technology. From the simulation results, it is found that LECTOR FGSRAM cell reduces 90.53% leakage power, 12% delay and 33.20% overall power consumption when compared to FGSRAM cell. A detailed comparison between FGSRAM cell and LECTOR FGSRAM cell performances has been reported during WRITE operation mode. **Application/ Improvements:** It is found that hybrid technique should be added along with LECTOR to improve the parameters.

Keywords: Floating Gate SRAM, High Speed, Hybrid Techniques, LECTOR, Low Leakage Power

1. Introduction

Memory caches occupy almost half of the total chip area and also consume a large amount of total power. SRAM is an essential building block of memory cache. Hence, better power reduction techniques are essential for the design of SRAM cell[1]. Leakage power dissipation is a major concern in modern days VLSI chip design. The main component of leakage power dissipation is sub-threshold leakage which occurs when PMOS and NMOS are switched off. Sub-threshold leakage current flows due to the diffusion of minority carriers; when the gate to source voltage is less than the threshold.

Various techniques are reported in the literature to address the leakage power dissipation issue in nanometer technology. Some of the commonly used techniques are a stack, sleep, sleep-stack, GALEOR, LECTOR, sleepy keeper, zigzag, zigzag keeper etc. In this paper combination of LECTOR and FGMOS has been used to achieve low leakage power and high speed. LECTOR technique has been used to reduce the leakage power dissipation of the SRAM[2–5] and FGMOS has been used to reduce the overall power consumption and delay of the circuit. When the floating gate is fully charged, the SRAM cell acts like a flash memory which is non-volatile in nature. On the other hand, when it is not charged it will act like a volatile SRAM cell.

From Figure 1, it has been observed that percentage of full chip area covered by the cache memory is increasing with technology scaling. Figure 2 shows that leakage power is increasing with the technology scaling.

2. Floating Gate MOSFET

FG MOSFET[6] is broadly utilized as flash memory. On the off chance that the FG is not charged it acts verging on like a typical MOSFET. FG MOSFET is totally encompassed by a seclusion layer that is the reason it can likewise be utilized as a part of non-unpredictable memory. A positive charge in the control gate makes a diversion in the

*Author for correspondence

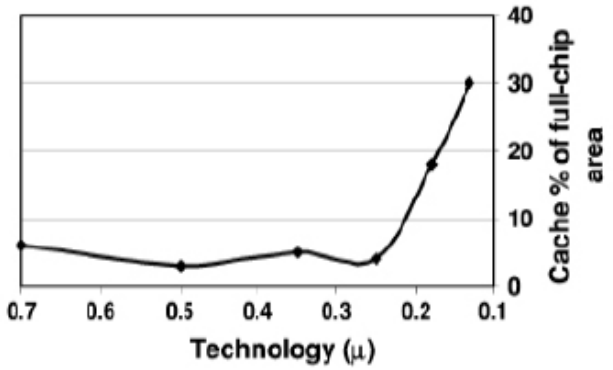

Figure 1. Technology vs cache % of full-chip area.

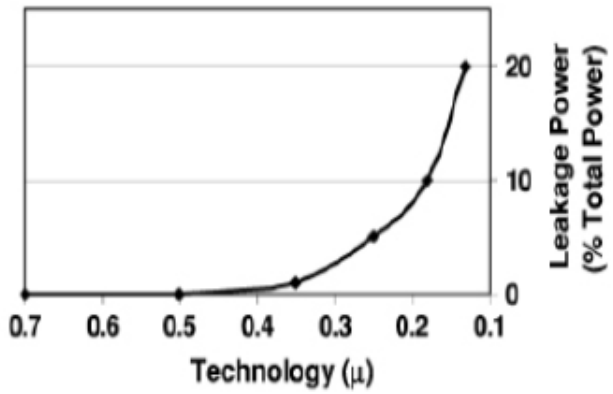

Figure 2. Technology vs leakage power.

p-substrate that forms a channel from source to deplete which is the current source. On contrary, if the control gate is charged negatively then this charge shields the channel area from the control gate and keeps the arrangement of a channel amongst source and deplete. Figure 3 demonstrates the constructional points of interest of floating gate MOSFET[7].

The voltage of the floating gate shown in Figure 3 is given by Equation (1)[6].

$$V_{FG} = \frac{\sum_{i=1}^{N} C_i V_i + C_{fd} V_{DS} + C_{fs} V_{SS} + C_{fb} V_{BS} + Q_{FG}}{C_T} \quad (1)$$

And the total capacitance is expressed by Equation (2)

$$C_T = \sum_{i=1}^{N} C_i + C_{fd} + C_{fs} + C_{fb} \quad (2)$$

where $C_1, C_2, C_3, \ldots, C_N$ are the information capacitances present in the middle of control gate and FG, C_{fd} is the capacitance present between channel and floating gate,

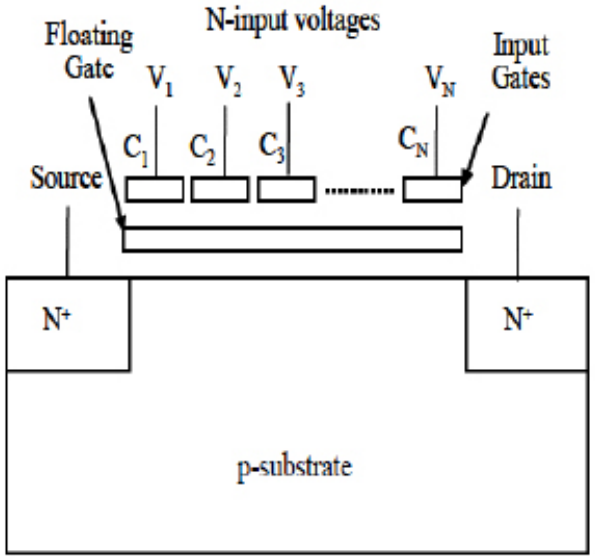

Figure 3. Floating gate MOS

C_{fs} is the capacitance between source and floating gate, and C_{fb} is the parasitic capacitance between substrate and floating gate. Q_{FG} is the residual charge which can be ignored during the manufacture procedure[8].

Therefore, Equation (1) can be reduced to Equation (3)

$$V_{FG} = \frac{\sum_{i=1}^{N} C_i V_i + C_{fd} V_{DS} + C_{fs} V_{SS} + C_{fb} V_{BS}}{C_T} \quad (3)$$

The drain currents in FGMOS for ohmic and saturation regions are given according to Equation (4) and Equation (5) respectively.

$$I_{DS}^{0} = Kn\left(\left(\left(\frac{\sum_{i=1}^{N} C_i V_i}{C_T}\right) - V_{ss} - V_T\right) V_{DS} - \frac{1}{2} V_{DS}^2\right) \quad (4)$$

$$I_{DS}^{s} = \frac{Kn}{2}\left(\left(\frac{\sum_{i=1}^{N} C_i V_i}{C_T}\right) - V_{ss} - V_T\right)^2 \quad (5)$$

where $K_n = \mu_n C_{ox}(W/L)$, and V_T is the threshold voltage of floating gate MOSFET. The N-channel N-input FGMOS transistor's symbol is shown in Figure 4 and the proposed FGSRAM is shown in Figure 5.

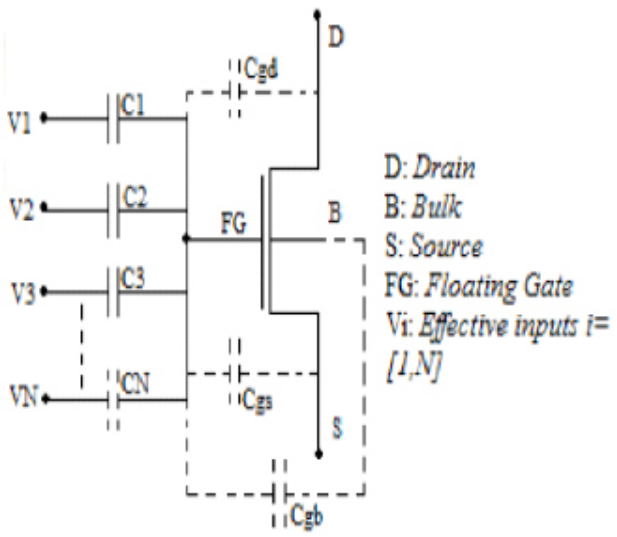

Figure 4. N-channel N-input FGMOS transistor.

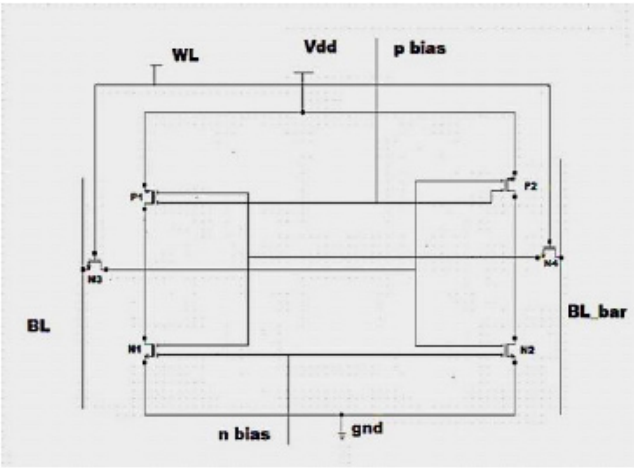

Figure 5. Proposed FGSRAM.

3. Lector Technique

In Figure 6, LCT_1 and LCT_2 are two leakage control transistors (LECTOR)[9,10]. This technique is used to make effective stacking from supply voltage to ground. Here, mainly more number of transistors is in off state between supply power rails. This causes reduction of leakage current.

The circuit configuration in the LECTOR approach ensures that one of the two leakage control transistors always operates near its cut-off region irrespective of the input voltage. According to LECTOR technique in a path between supply and ground having more than one transistor is less leaky than the path having only one transistor.

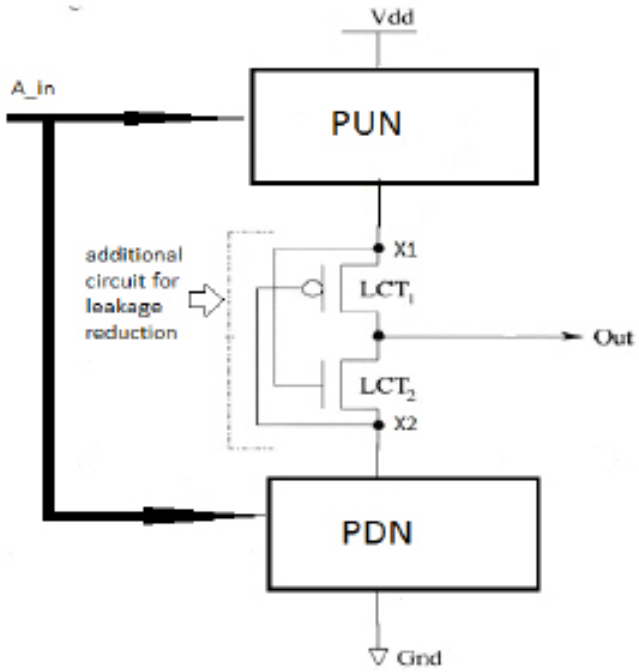

Figure 6. LECTOR technique is applied in between pull up and pull down network.

Thus, the LECTOR approach leads to a current limited resistive path between the supply voltages to reduce the leakage power dissipation through the lector circuit.

In Figure 6, LCT_1 is placed in between pull up network and output and is controlled by the potential at x_2. LCT_2 is placed in between pull down network and output and is controlled by the potential at x_2. In this circuit configuration one LCT is always in the cut-off region and in turn increases the resistance from supply voltage to ground and due to this leakage current is highly reduced.

4. Simulation Results and Performance Analysis

Figure 7, Figure 8 and Figure 9 show the proposed LECTOR FGSRAM circuit, transient response of FGSRAM and transient response of FGLECTOR SRAM respectively.

4.1 Static Noise Margin (SNM)

The static noise margin can be determined from the parallel cell memory solidness which is obtained by making and reflecting the qualities of inverter. The greatest square between the two inverters as steadiness of a specific SRAM is contrarily corresponding to the spillage current.

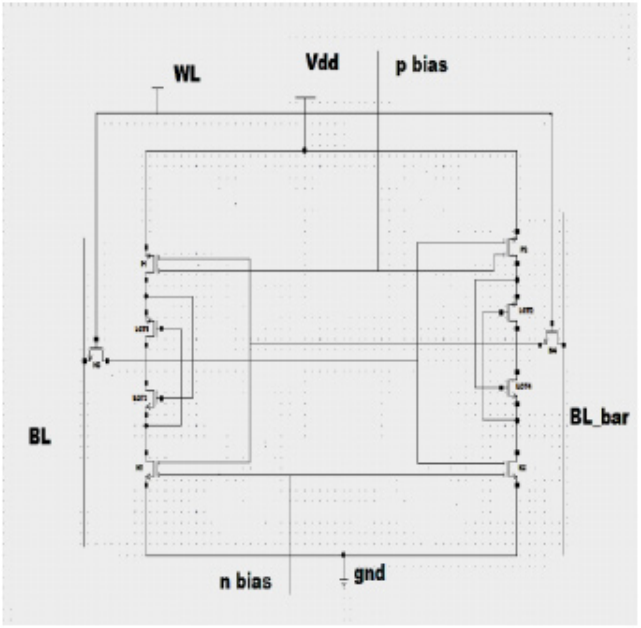

Figure 7. Proposed LECTOR FGSRAM.

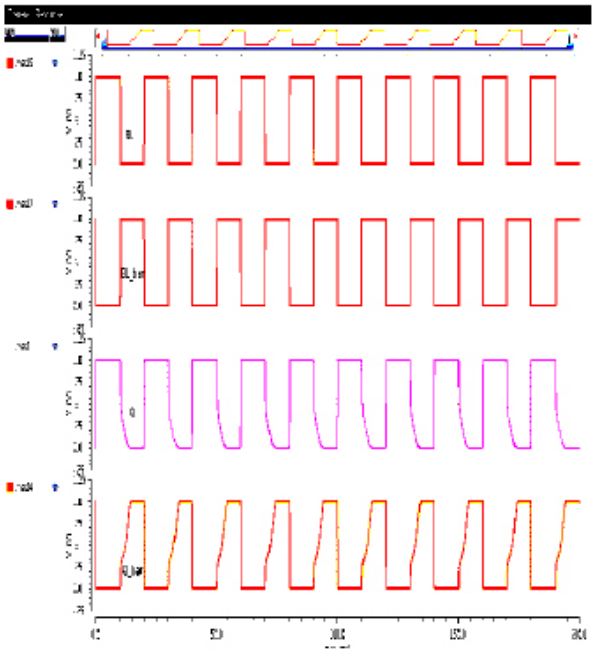

Figure 8. Transient response of FGSRAM.

So, a bigger SNM is required for stable SRAM operation. To flip the cells information of the SRAM cell, a common voltage is required at the inner hubs of the SRAM which can be measured from the SNM in Figure 9. By switching the draw up proportion and draw down proportion the solidness of SRAM cell can likewise be changed. The

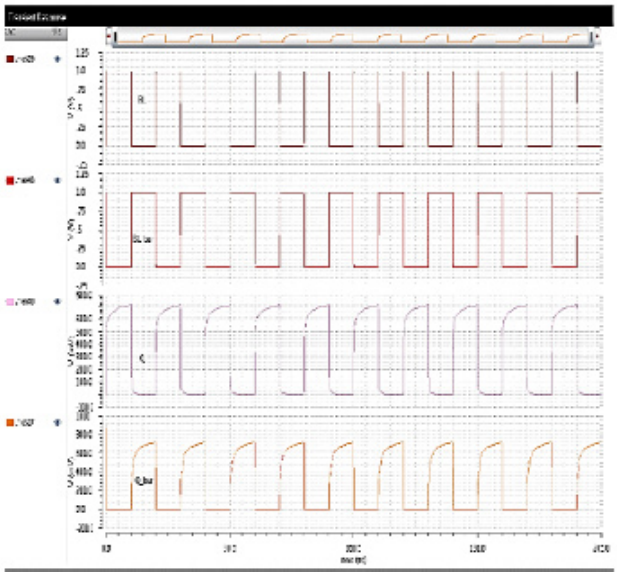

Figure 9. Transient response of FGLECTOR.

proportion between sizes of the driver transistor to the lower transistor can be mentioned as the cell ratio. During the READ operation mode, pull up ratio is only a ratio between sizes of the low transistor to the entrance transistor along with WRITE operation.

For READ stability; Pull up Ratio (PR) is taken more than 1.2 and for WRITE stability; Cell Ratio (CR) is taken less than 1.89. In this paper, transistor size draw up proportion has been taken as 1.25 and cell proportion as 0.725.

Figure 10 and Figure 11 show the WRITE SNMs of FGSRAM and FGLECTOR SRAM. It can be observed that there is smoothness in the butterfly curve obtained in FGLECTOR technique over FGSRAM without compromising the performance.

From Table 1, it is observed that LECTOR and floating gate based SRAM cell achieves 90.53% and 6.2% reduction in leakage power and delay respectively during WRITE 0 operation. Table 2 shows that using LECTOR technique, 90.53% leakage power and 17.6% delay is reduced for WRITE 1 operation.

From Table 3, it is observed that using LECTOR technique along with FGSRAM cell leakage power is reduced by 90.53% and delay is reduced by 17.72% during READ 1 operation. For READ 0 operation mode, 5.24% delay is reduced which is shown in Table 4.

From Table 5 and 6, it can be observed that using LECTOR method, it can reduce 62.61% WRITE power consumption and 3.8% READ power consumption compare to FGSRAM.

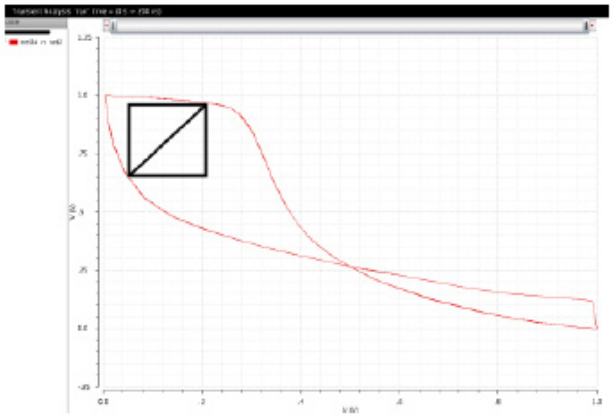

Figure 10. WRITE SNM of FGSRAM

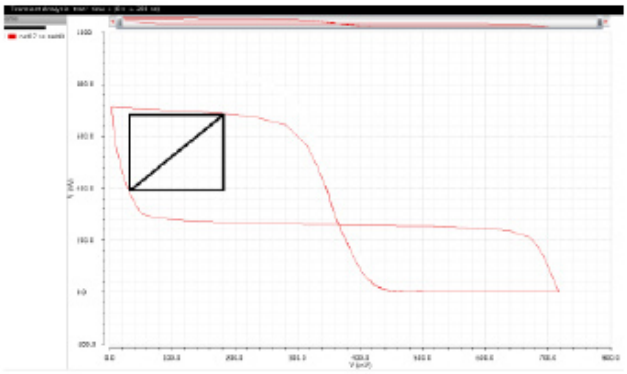

Figure 11. WRITE SNM of FGLECTOR.

Table 1. WRITE 0 operation

SRAM cell	Leakage Power	Delay
FG	3.36 nW	296.9 pS
FGLECTOR	318.6 pW	278.5 pS

Table 2. WRITE 1 operation

SRAM cell	Leakage Power	Delay
FG	3.365 nW	152.6 pS
FGLECTOR	318.6 pW	125.77 pS

Table 3. READ 0 operation

SRAM Cell	Leakage Power	Delay
FG	3.366 nW	297.6 pS
FGLECTOR	318.6 pW	282.08 pS

Table 4. READ 1 operation

SRAM Cell	Leakage Power	Delay
FG	3.365 nW	153.2 pS
FGLECTOR	318.6 pW	126.04 pS

Table 5. WRITE power consumption

SRAM Cell	Power Consumption
FG	228.5 nW
FGLECTOR	85.43 nw

Table 6. READ power consumption.

SRAM Cell	Power Consumption
FG	3.909 uW
FGLECTOR	3.76 uW

Table 7. WRITE SNM

SRAM Cell	SNM
FG	424.2 mV
FGLECTOR	395.9 mV

Table 8. READ SNM

SRAM Cell	SNM
FG	247.4 mV
FGLECTOR	395.9 mV

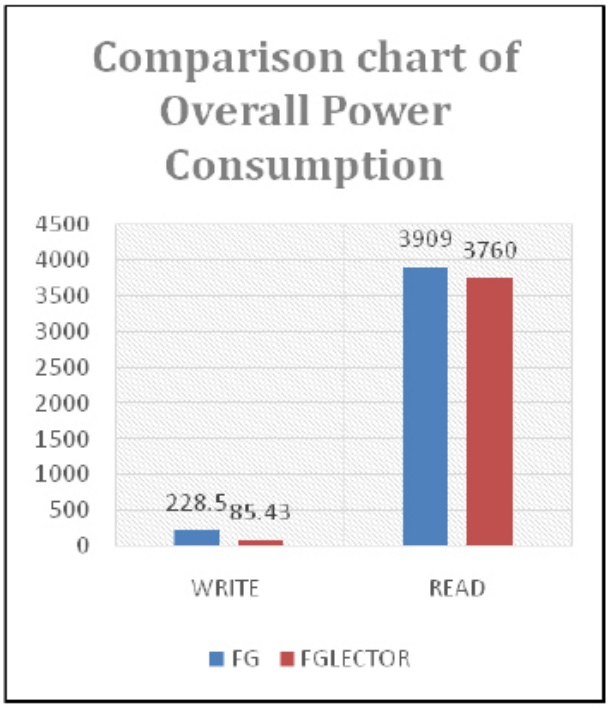

Figure 12. Power consumption comparison between FG and FGLECTOR.

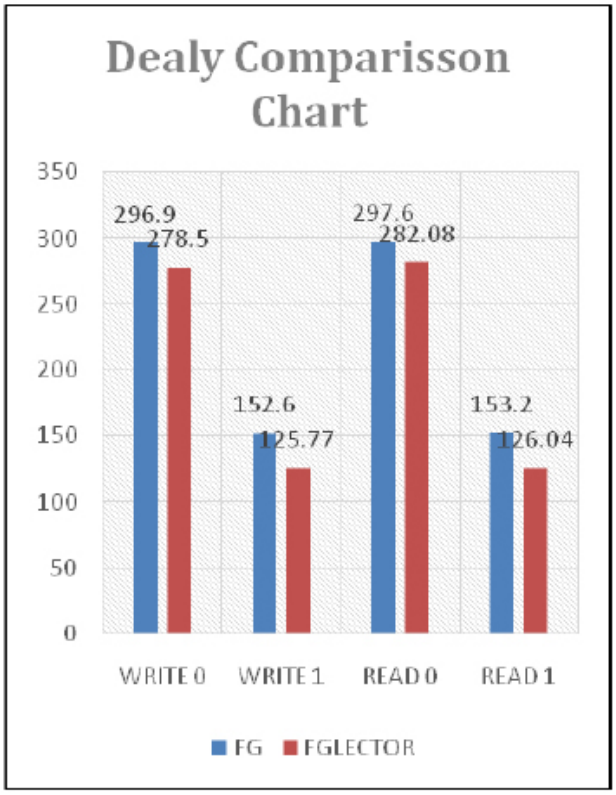

Figure 13. Delay comparison between FG and FGLECTOR.

From Table 7 and 8, it can be observed that using LECTOR method 37.5% READ stability is increased.

Figure 12 and Figure 13 shows accordingly power consumption and delay comparison chart. From the Figures it can be inferred that there is a significant reduction in both power consumption and delay during READ and WRITE operations.

5. Conclusion

The paper proposes a low power high speed SRAM cell based on floating gate and LECTOR techniques. The simulation of the proposed design is realized on 45 nm standard CMOS process technology using Cadence EDA tool. The performance analysis was carried out for different techniques. Simulation results show that LECTOR technique efficiently reduces 90.53% leakage power, 12% delay and 33.20% overall power consumption compare to FGSRAM. Table 7 represents some drawback of the design that 6.67% stability is decreased. So, the hybrid technique should be added along with LECTOR to improve the parameters.

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