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Design and Comparative Analysis of Domino Logic Styles

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Abstract

Background/Objective: To design the AND, OR type circuits based on foot based and foot-less based gate domino logic and compare the results. **Methods/Statistics:** Nowadays VLSI circuits are expected to operate with low power, high speed, less area and noise tolerance. The major challenge in VLSI circuits is to obtain high performance. There are several digital logic techniques available viz. pseudo static CMOS, pass-transistor logic, complementary pass-transistor logic, GDI, dynamic CMOS logic, domino CMOS logic, which can be used to achieve high performance circuits. **Findings:** Static CMOS circuits have both pull down and pull up networks, but the disadvantage is, total number of transistors in the circuit is more. The dynamic logic circuits overcome the disadvantage of static complementary MOS. On the other side dynamic logic suffers from charge leakage, charge sharing and noise sensitivity, due to sub-threshold leakage current flow in the Pull Down Network (PDN), called stacking effect. When we scale down the technology, these effects will also get increased.

Keywords: Footed, Foot-Less Domino, Power Dissipation

1. Introduction

Earlier, VLSI circuits are designed by using static CMOS logic using logic 2n transistors having the pull up network and pull down network. The basic circuit design is shown in Figure 1. This method is useful to design all type of circuits, but the drawbacks as the number of transistors increases, more the power dissipation and occupy larger area.

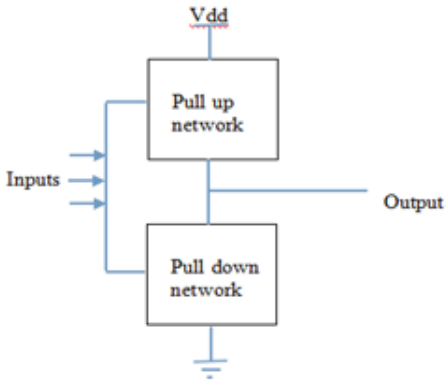

Figure 1. Static CMOS logic.

To overcome the drawbacks of static CMOS logic, dynamic CMOS logic is introduced. In this logic n+2 transistors are used. The basic circuit design is shown in Figure 2. It is operated in two phases: Precharge phase and evaluation phase. In Precharge phase, clk = 0, inputs are varying or not varying; output is high. In evaluation phase, clk = 1, observe the output by varying the inputs; in reduces the area and transistors, but it suffers from charge leakage and charge sharing problems[1].

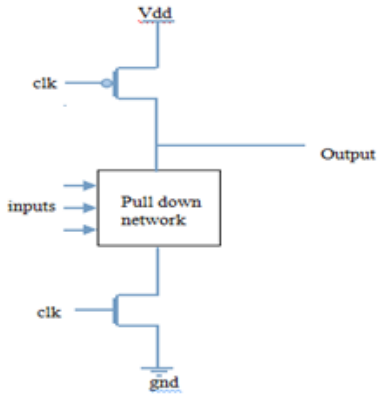

Figure 2. Dynamic CMOS logic.

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In this charge, sharing occurs when the primary input of pull down network is active and remains low that time the output capacitance is shared with input capacitance. In this charge leakage occurs when the clk = 1; at that time output is high and pull down network inputs is low; during that time, output capacitance leaks some charge through PDN due to sub-threshold leakage.

2. Domino Logic

In this we use the static CMOS inverter at output of dynamic CMOS logic. The basic circuit design is shown in Figure 3. Operation is same as dynamic CMOS logic, but output is changed. In pre charge phase, when clk = 0, PDN is ON or OFF the dynamic node is high and output is low. In the evaluation phase clk = 1, by varying the PDN inputs and verify the output. It has less power dissipation and high speed, but in this implements only non-inverting logic.

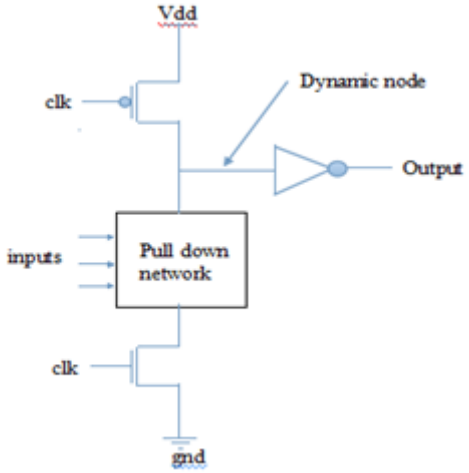

Figure 3. DOMINO CMOS logic.

Domino logic can be implemented in foot based gate and footless based gate. Foot based gate means NMOS transistor is connected to bottom of the PDN, it is same as Figure 3, footless based gate means remove the NMOS transistor at PDN bottom, it is shown in Figure 4. Footless based gates have more power dissipation and leakage current compared to the footed[2].

Domino logic can be classified into[3]:

- Keeper implementation.
- Precharge internal nodes.
- Raising source voltage.
- Complementary p-type network.

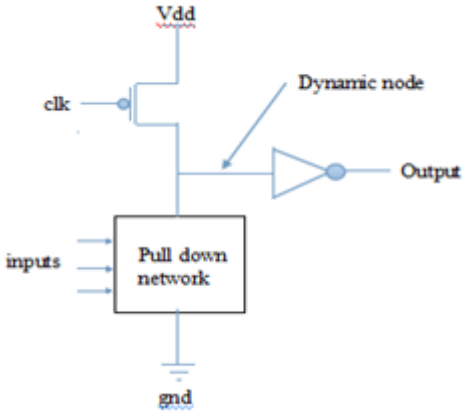

Figure 4. Footless based domino.

2.1 Keeper Implementation

In the evaluation phase PDN is going low and some charge leakage occurs and it is known as charge leakage. To reduce the charge leakage, keeper transistor[4] is employed (Figure 5).

This keeper restores the voltage at dynamic node; due to this, dynamic node is always high but in the evaluation phase when PDN is active there is a direct path between vdd and ground; but DC power consumption will increased. To decrease DC power consumption, feedback keeper transistor[5] is employed (Figure 6). Using of this technique improves noise immunity.

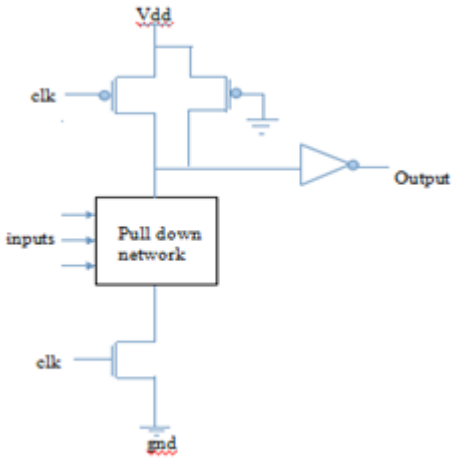

Figure 5. Keeper implementation.

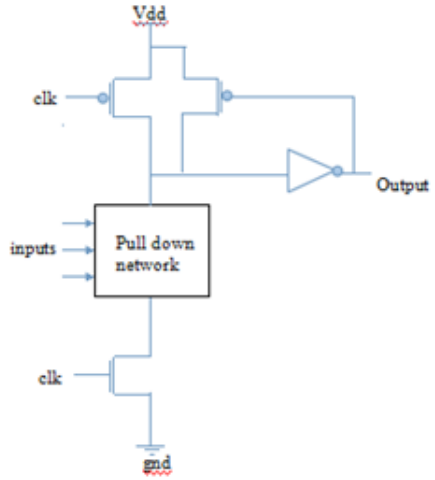

Figure 6. Feedback keeper transistor.

2.2 Precharge Internal Nodes

In the circuit, when the dynamic node is high, at that time PDN conducts few inputs and output capacitance is shared with input capacitance[6]. To reduce the charge sharing problem, consider the three input and gate, Precharge the internal nodes, it is shown in Figure 7. Due to this decrease discharging time and dynamic power consumption.

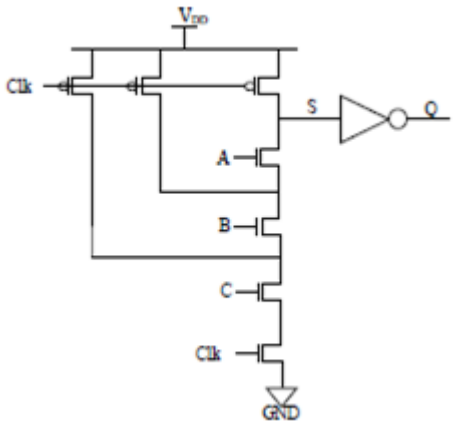

Figure 7. Precharge internal nodes.

2.3 Raising Source Voltage

In this method to increase noise tolerance of the circuits by increasing source at PDN. In this we are using pull-up transistor at bottom PDN[7], it is shown in Figure 8. In this design by varying the size of pull up transistor to adjust the threshold voltage of the PDN.

But the drawback is the DC power consumption is increased. To overcome the drawback, pull-up is replaced by NMOS transistor[8] (Figure 9). But when the PDN is not conducted, at time dynamic node is high and NMOS is on, there is a direct path between vdd and ground, which increases the power consumption.

To decrease the power consumption, mirror technique[9] is introduced, it is same as NMOS pull up and PDN again connected to bottom PDN (Figure 10). But in the evaluation phase, dynamic node to ground path is increased.

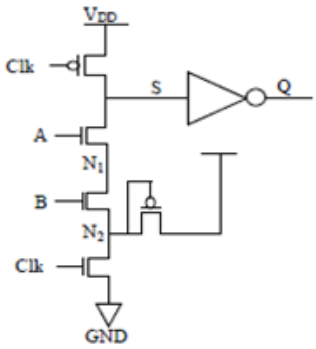

Figure 8. PMOS pull-up technique.

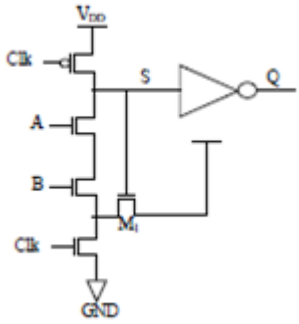

Figure 9. NMOS pull-up technique.

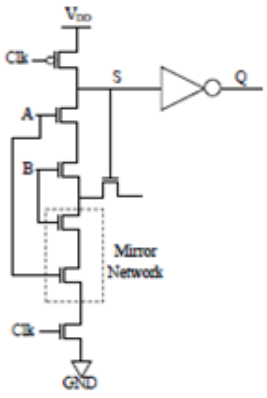

Figure 10. Mirror technique.

2.4 Complementary P-Type Network

It is same as static CMOS logic and add PMOS transistor to pull-up network parallel, NMOS transistor to bottom PDN.

In this technique eliminate the dynamic node when clk = 1 (evaluation phase), when clk = 1, it operates as a normal CMOS logic, when clk = 0, it operates as a domino logic (Figure 11), but it is not supported for OR type circuits[10].

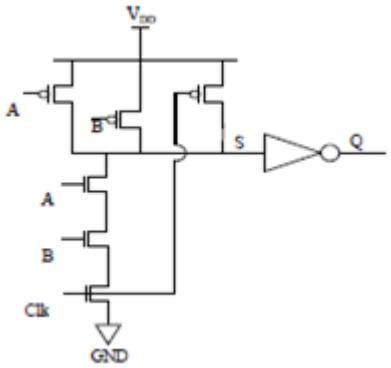

Figure 11. Complementary p-type network.

3. CMOS Implementation of Domino Logic

In the domino logic we are designed the AND, OR gates by using foot based gate[11] and foot-less based gate[12]. In this paper given the comparison footed and foot-less based gates, below shown the foot-LESS based AND, OR circuits[13], shown in Figure 12 and Figure 13. Footed based gates[14] are shown in Figure 14 and Figure 15. In this process we are taken the four inputs, foot-less based circuits using implemented by 8-transistors and foot based circuits are implemented by 9-transistors. In the AND circuits when clk = 0 (Pre charge phase), dynamic node is high, it is foot-less based on the inputs output will varied. It is in footed based circuit output is low in Precharge phase and when clk = 1 (evaluation phase) based on the inputs output will varied. Based on results we can observe the waveforms of foot-less and foot based circuits and also observe the power dissipation. In the AND gate power dissipation is little difference between two circuits, in the OR type circuits large difference in foot-less and foot based circuits. Simulation results will be shown in Figure 16, Figure 17, comparison of power dissipation both circuits will be shown in Table 1.

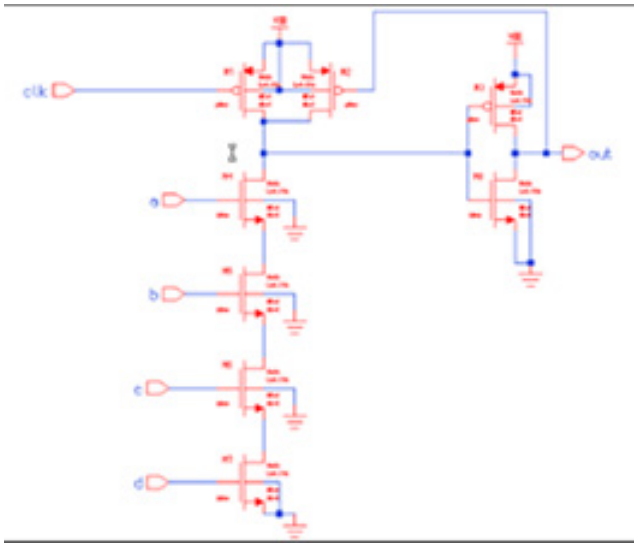

Figure 12. Foot-less AND gate.

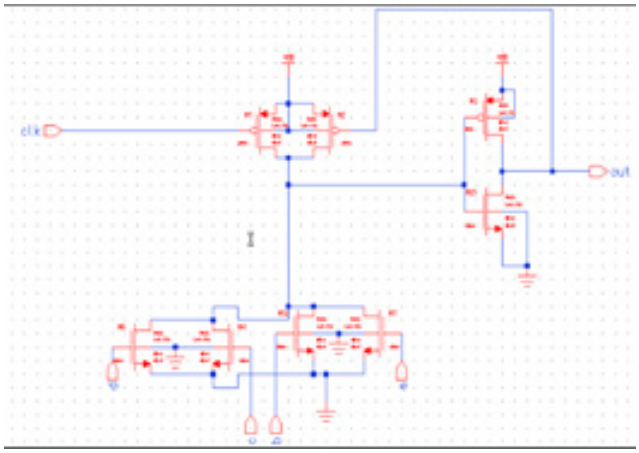

Figure 13. Foot-less OR gate.

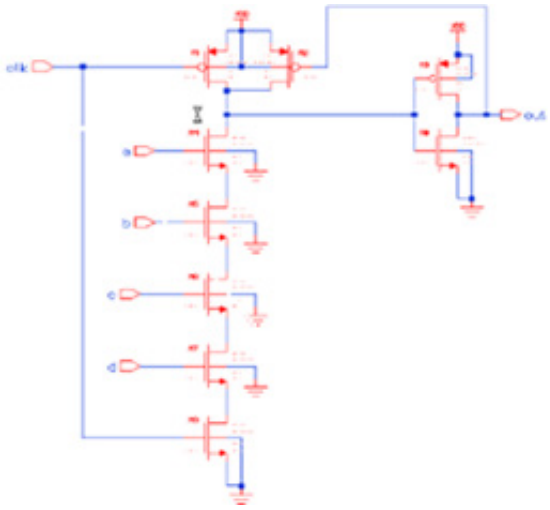

Figure 14. Foot based AND gate.

Table 1. Comparison of foot and foot-less

Design type	Supply voltage (V)	AND gate power dissipation (pw)	OR gate power dissipation (pw)
Foot based	1	332.76	566.72
Foot less based	1	355.01	3353

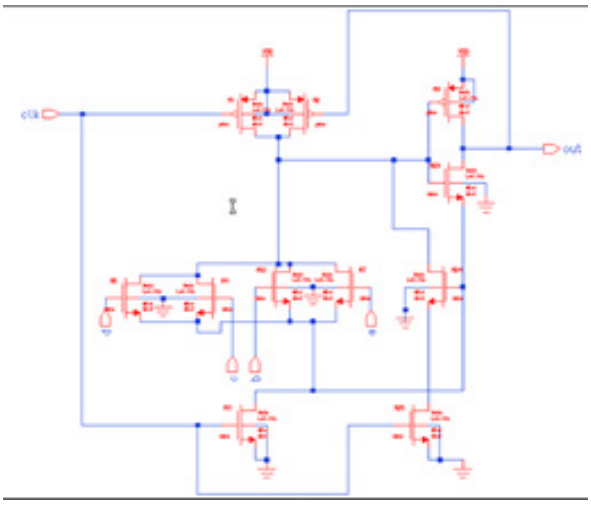

Figure 15. Foot based OR gate.

4. Conclusion

Based on the simulation results, foot-less based circuits have the more power dissipation compared to foot based circuits; footed circuits show better performance. In the future, ALU will be designed, based on the footed and foot-less domino logic and a comparative study will be made.

5. Acknowledgment

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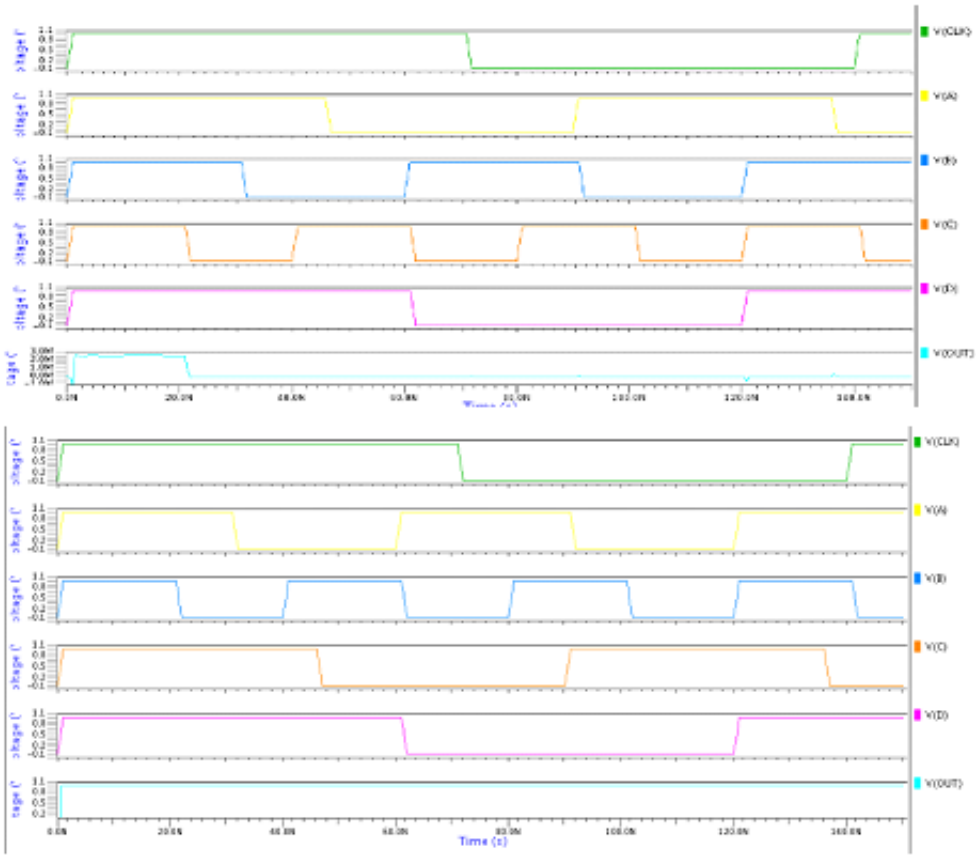

Figure 16. Transient response of foot-less AND, OR circuits.

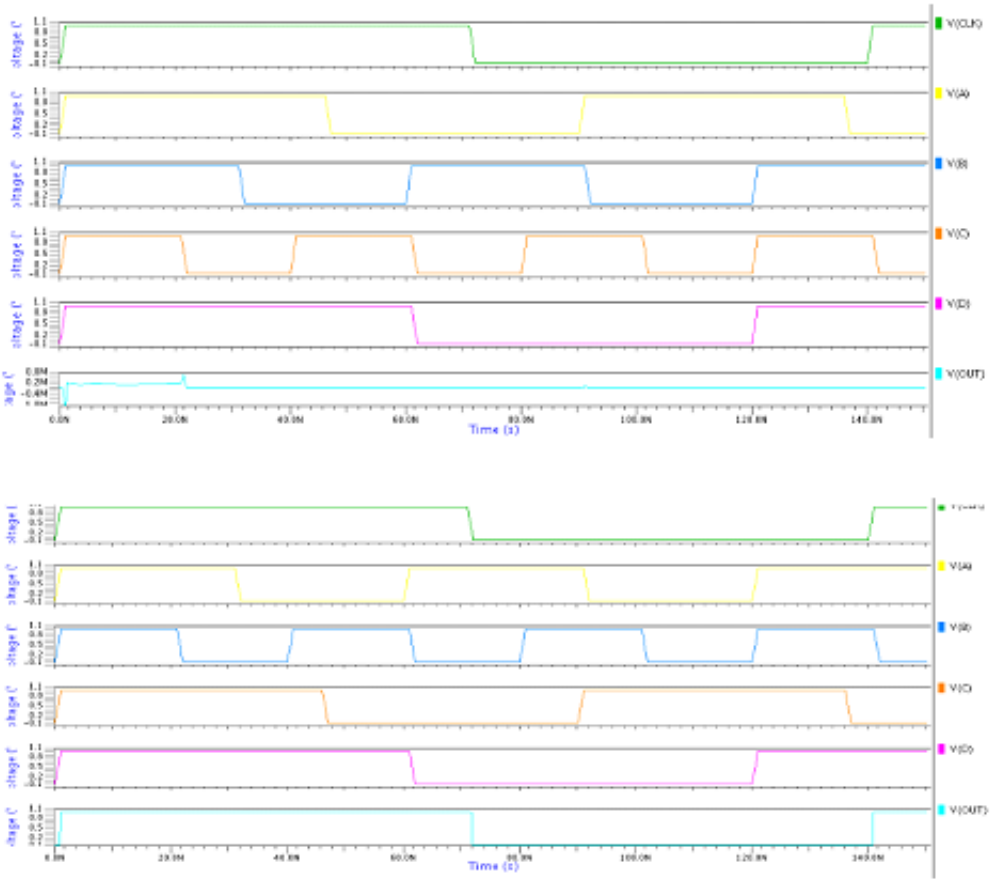

Figure 17. Transient response of foot based AND, OR circuits.

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