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Low Power and High Speed PB-CAM with XNOR-NAND Parameter Comparison Circuit

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Abstract

Objectives: Low power consumption, high-speed and low-cost are the major important needs in several applications like Asynchronous Transfer Mode (ATM) and Giga-bit Ethernet networks. To achieve high-speed parallel data comparisons in internet routers PB-CAM is the one of best hardware approaches. In the present work, PB-CAM is modified for improving performance of CAM architecture. **Methods/Statistical Analysis:** In PB-CAM unit the main building blocks of the process is parameter extractor, parameter comparison circuit and CAM cell. The PB-CAM is faster and low-power consumption than the traditional CAM. The PB-CAM unit implemented by 180nm, 90nm and 45nm CMOS technology in Cadence. The parameter-extractor and static-parameter-comparison circuits implemented in 180nm, 90nm and 45nm CMOS technology. **Findings:** The power consumption of the proposed Parameter-Comparison circuit using XNOR-NAND CMOS logic is 0.02135uW at a supply voltage of 0.45V in 45nm CMOS technology for a 4x4 (4-bits of stored parameter-extracted data and 4-bits of input parameter-extracted data) size parameter comparison data at 10-30MHz. For 15-bit input data, the PB-CAM with proposed parameter comparison circuit is consuming an average power of 129.1uW at a supply of 0.9V and a frequency of 10-30MHz. The results show that the PB-CAM unit using proposed parameter comparison circuit is faster, low-power consumption and low-cost than the PB-CAM with static parameter comparison circuit. **Application/Improvements:** PB-CAM circuit used in high-speed look-up-tables (LUTs), ATMs, routers and etc. In future, further advancements can be done in PB-CAM unit by combining different techniques such as match-line-sense-amplifier, ones-count, block-XOR, parity-bit to achieve low-power, low-cost and high-speed search and read operations in network routers.

Keywords: ATM, Cadence, CAM, Ethernet, High-Speed, Low-Cost, Low Power, Match-Line, PB-CAM, Routers

1. Introduction

Numerous growths in internet users and the popularity of increasing bandwidth in real time applications results in demand for very rapid networks. Internet is amalgamation of switches and routers, which used to process data and forward towards their destination. Data is in the form of packets and each one packet having a payload and a header. The header has information of sender (source) address, receiver (destination) address, length of the data, serial number and packet data type. Based on the information available in header of data-packet, network-switch transfers input data-packet to output terminal. Router is a most elegant switch[1], which defines a temporary routing path between the source and destination to allow incoming data packets. To update tables in routers (routing tables) they can communicate with one another. Mostly, the optical fiber is used to transfer the data from one router to another. Because of vast advantages of optical fiber in communication networks, Wavelength Division Multiplexing (WDM) has phenomenal increase in the data transfer rates[2]. Hence, router needs up gradation to use the full performance of optical fiber technology[3]. In router or network-switch, LUT is one of the time-consuming processes.

Internet Protocols (IPs) namely IPv4 and IPv6, IPv4 only supports 32-bit IP addresses[2]. Due to usage growth in number of internet users, shortage of IPv4 addresses had come to existence. Therefore, IPv6 protocol introduced and it supports 128-bit addresses. IPv4 replaced gradually by IPv6. While migrating from IPv4 to IPv6, there are

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different design considerations on LUTs and packet forwarding. In IPv6 network-nodes are large in number and thus increasing the size of word and routing table capacity in packet forwarding[3,4]. First, the word size will increase from IPv4 (104-bits) to IPv6 (296-bits), hence it reduces the speed of the LUTs. Second, most of the packets were processed by multiple LUTs. Hence, a large delay can significantly reduce the policy lookups speed.

Software algorithms for LUTs radix-tree are relatively slow[4]. In memory access a hash-function can be used in LUTs, and its worst case search-time, it always depends on the hash-function and size of the LUT. Hence it is awkward than the tree searching algorithms. Therefore, the LUTs which were implemented in software for different network layers are now going to replace by hardware to enhance the performance. The most powerful hardware to function as LUT is a Content Addressable Memory (CAM). A CAM is a computational logic memory circuit, which is used to compare the data simultaneously. Mostly CAM is used in Asynchronous Transfer Mode (ATM), internet-routers, look-up-tables (LUT), data compression, tag directories, switches, associative computing, communication networks and Gigabit Ethernet[5]. CAMs are generally classified into two types: (i) Binary-CAM and (ii) Ternary-CAM (TCAM)[6]. A Binary-CAM can be used to search and store only binary data, i.e. 0s and 1s, whereas TCAM can be used to search and store ternary states i.e. 1, 0 and X where 'X' is used for partial matching of the data. [Figure 1] illustrates the conceptual block diagram of traditional CAM.

2. Concept of PB-CAM

The memory-organisation of traditional CAM consists of valid-bit-field and data-memory[1]. In general CAM consists of valid-bit-field, data-memory, address-priority-encoder, word-match-circuit, bitline-precharger and address-decoder.

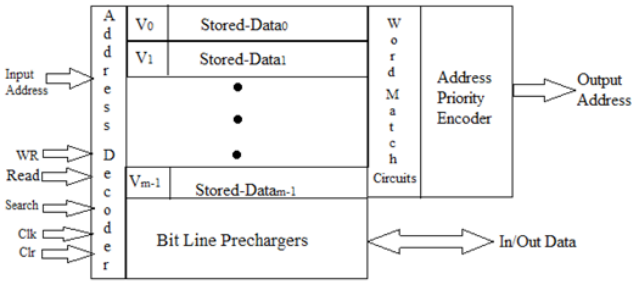

Figure 1. Block diagram of traditional CAM[1].

PB-CAM composed of the parameter-extractor, parameter-memory and the data-memory as shown in [Figure 2]. In write operation parameter-extractor is used to extract the parameter of input data, parameter-memory is used to store the extracted parameter of the input data and the data-memory is used to store the input data with stored parameter in PB-CAM respectively. In data search operation, in order to reduce time consumption for comparison processes[1], it has classified as two comparison operations which are listed below.

i) Parameter extractor is used to extract the parameter of input-data and this extracted parameter is compared with the stored parameters in the parameter-memory by parameter comparison circuit.
ii) If it matches in the first process then the input-data compared with the stored data in the data-memory, and later on if it is matched with stored data then specified input data of parameter is identified and send to output.

Here pre-computation is simply the parameter comparison operation. The operation of ones-count PB-CAM[7] is shown in [Figure 3].

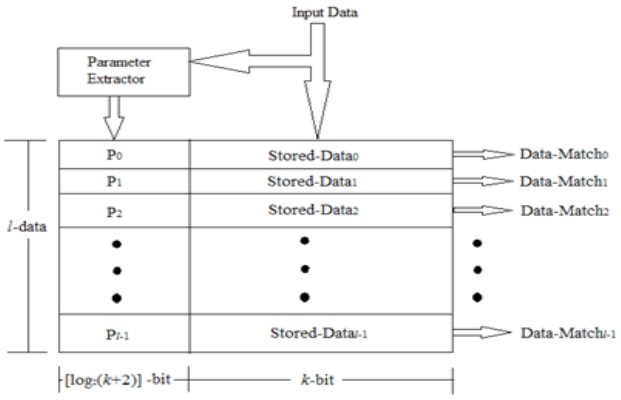

Figure 2. PB-CAM memory-organization[1].

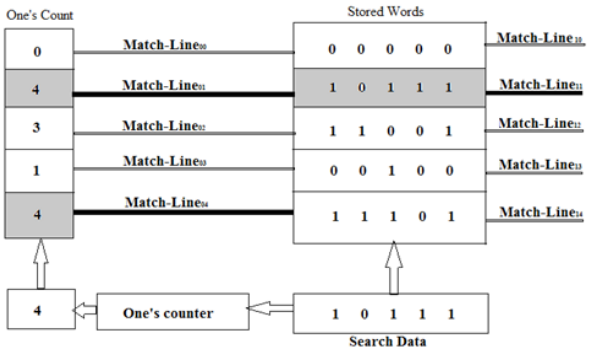

Figure 3. Ones-count PB-CAM conceptual view[7].

3. Concept of Parameter Extractor

In Ones-count PB-CAM the parameter extractor is used to extract the parameters of the input-data as shown in [Figure 4]. These extracted parameters are used to store and/or compare the parameters in the parameter-memory and parameter comparison circuit. The parameter extractor output depends on the number of ones present in the input-data of the parameter extractor. For *k*- bit input data there are ($k + 1$) kinds of ones count (0 to *k* ones-count). The minimum required input-data for the parameter extractor is $log_2(k + 2)$. The size of the CAM is *l* words by *k* bits, i.e. ($k * l$).

15-bit input-data is fed to the parameter extractor and the output obtained is of 4-bit parameter size. The transient response of parameter extractor is as shown in [Figure 5].

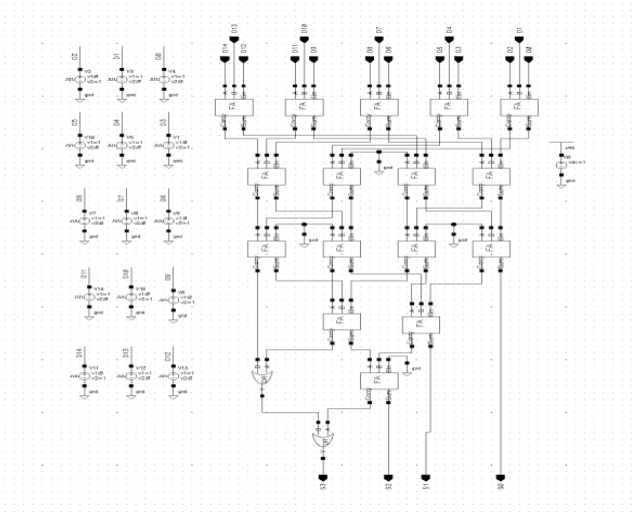

Figure 4. Implementation of parameter extractor circuit using 90nm CMOS technology.

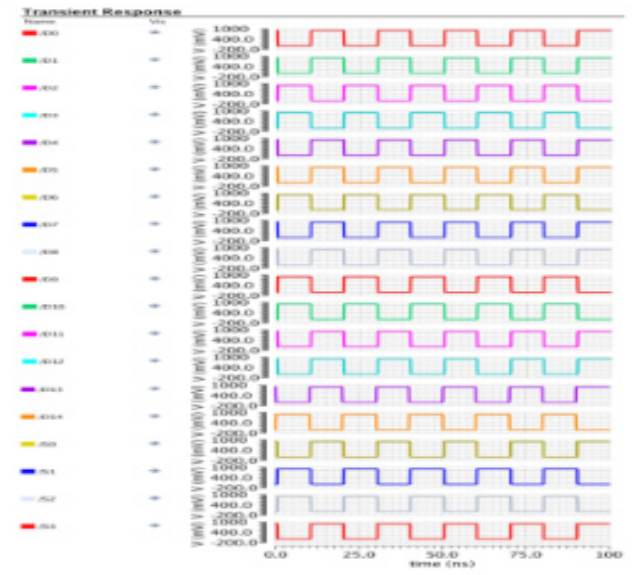

Figure 5. Transient response of parameter extractor circuit using 90nm CMOS technology.

4. Concept of CAM Cell

Two basic functions processed by CAM cells are bit-comparison (specific to CAM) and bit-storage (like in RAM).

Table 1. Average Probabilities and total number of data related to the same parameters by using ones-count parameter extractor function[1]

Parameter		Total number of data related to the respective parameter	The average probability
1111	15	Valid bit	
1110	14	1	0.01%
1101	13	14	0.09%
1100	12	91	0.56%
1011	11	364	2.22%
1010	10	1001	6.11%
1001	9	2002	12.22%
1000	8	3003	18.33%
0111	7	3432	20.95%
0110	6	3003	18.33%
0101	5	2002	12.22%
0100	4	1001	6.11%
0011	3	364	2.22%
0010	2	91	0.56%
0001	1	14	0.09%
0000	0	1	0.01%

One of the traditional CAM cells namely 9-transistor (9T) as shown in Figure 6. It consists of a back-to-back connected CMOS inverter and the output of CAM cell connected to Match-Line. Each CAM cell consists of write-line (WL), bit-line (BL) and bit-line-bar ($\overline{BL}$). Where WL used to control the CAM cell for data writing and searching (comparison) operations.

During data-write-operation WL is high (logic-1), then it turns ON both the pull-up nMOS transistors, which connected to WL , then it leads BL and $\overline{BL}$ lines

get connected to back-to-back inverter. The whole process constitutes data-write-operation in the CAM cell.

In data-comparison operation WL is low (i.e. logic-0), then the pull-up nMOS transistors, which connected to WL will turned OFF, Therefore BL and $\overline{BL}$ lines are not connected to the back-to-back inverter. Thus BL and $\overline{BL}$ signals are directly connected to the sources of pull-down nMOS transistors respectively. One of the inverter's output from back-to-back connected inverter is connected to one of the pull-down nMOS transistor's gate and another inverter of back-to-back connected inverter output is connected to second pull-down nMOS transistor gate[8-11], this operation shown in Table 2. The 9T CAM cell and its transient response is as shown in [Figure 6] and [Figure 7] respectively.

PB-CAM cell has 7-transistors (7T), which used in Ones-count PB-CAM circuit. 7T PB-CAM proposed[1]. [Figure 8] shows the 7T PB-CAM cell implementation using 90nm CMOS technology and Figure.8 represents its corresponding transient response. This 7T PB-CAM cell consists of a back-to-back connected CMOS inverters and the output of CAM cell is connected to Match-Line. At the Match-Line two nMOS transistors are connected in series. Pull-up nMOS transistor's gate is connected to output of back-to-back inverters and whereas pull-down nMOS transistor's gate is connected to Bit-Line (BL $\overline{BL}$), these two nMOS transistors works on NAND operation[8], as shown in Table 3. The output waveform of 7T PB-CAM is as shown in [Figure 9].

Table 2. Operation of 9T CAM cell[1]

BLi	Qi	~BLi	~Qi	CAM cell
0	0	1	1	Floating
0	1	1	0	0
1	0	0	1	0
1	1	0	0	Floating

Table 3. Operation of 7T PB-CAM cell[1]

BLi	Qi	~Qi	PB-CAM cell
0	0	1	Floating
0	1	0	Floating
1	0	1	0
1	1	0	Floating

5. Concept of Parameter Comparison Unit

5.1 Static Parameter Comparison Circuit

Static Parameter Comparison (PC) circuit proposed by[1]. This static PC used to compare the extracted and stored parameters by the parameter-extractor in the PB-CAM.

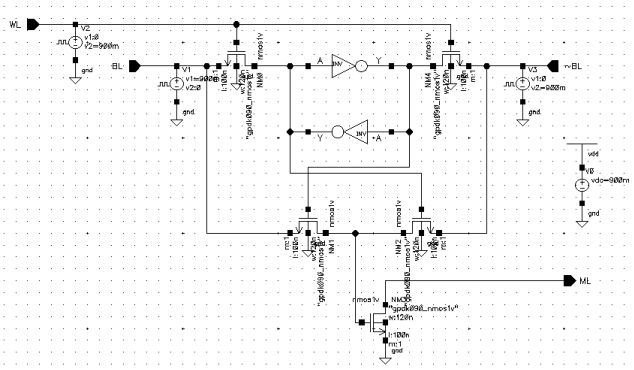

Figure 6. Implementation of 9T CAM cell using CMOS 90nm technology.

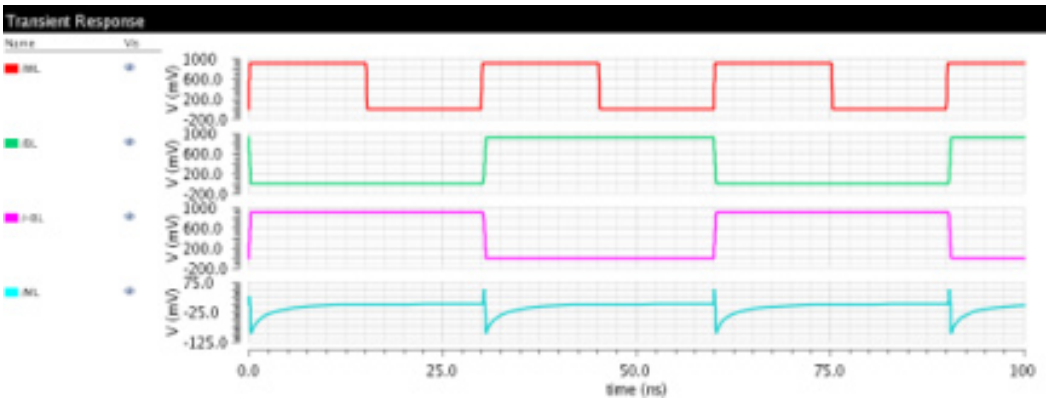

Figure 7. Transient response of 9T CAM cell using 90nm CMOS technology.

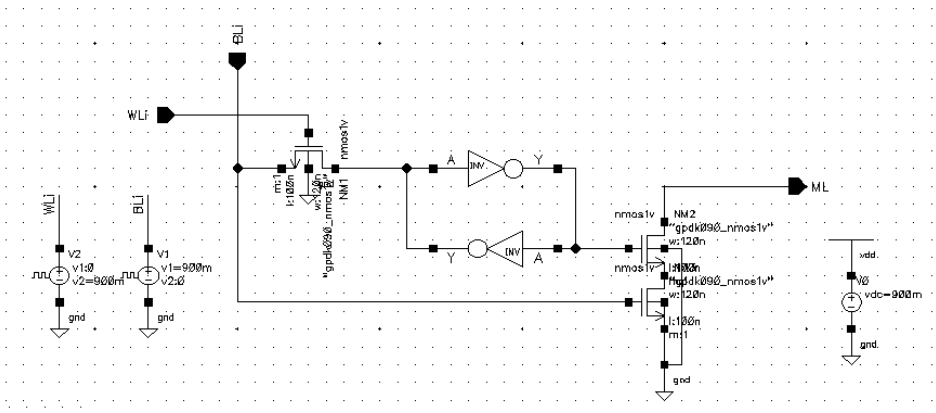

Figure 8. Implementation of 7T PB-CAM cell using CMOS 90nm technology.

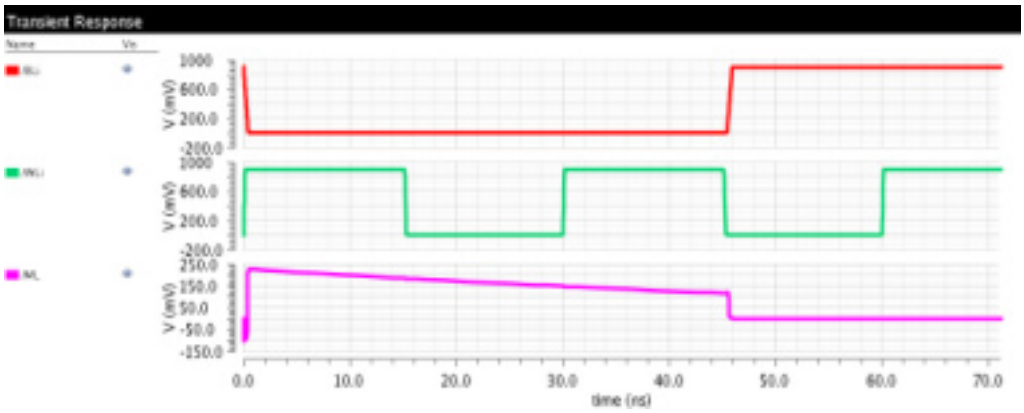

Figure 9. Transient response of 7T CAM cell using 90nm CMOS technology.

[Figure 10] shows the static parameter comparison circuit for 4-bit parameter. It has less speed comparison process and power-consumption is more when compared to our proposed parameter comparison circuit. For 10-30MHz frequency the average power consumption in CMOS 45nm technology is 0.03234uW at a supply voltage of 0.45V. The output waveform is as shown in [Figure 11].

5.2 Proposed Parameter Comparison Circuit

Parameter comparison circuit is mainly used for comparison of input and stored parameters of data in the PB-CAM. Our proposed parameter comparison circuit works on the basis of XNOR-NAND circuit and also Parameter Comparison circuit gives inverted output. i.e., if the parameter of stored data and parameter of new input data are matches, then the Parameter Comparison circuit gives output as 'logic-0' (Low). If the parameter of stored data and parameter of new input data are not matches, then the Parameter Comparison circuit gives output as 'logic-1' (High). The proposed parameter comparison circuit and its transient analysis is as shown in [Figure 12] and [Figure 13] respectively.

5.2.1 Mathematical Analysis of Proposed Parameter Comparison Unit

$$V = \overline{\{[sl(n-1) \odot bl(n-1)] * [sl(n-2) \odot bl(n-2)] \ldots [sl(0) \odot bl(0)]\}}$$

$$V = \overline{\{[sl(n) \odot bl(n)]\}}$$

Where sl = search-line.

bl = bit-line.

$sl(n-1)$ = n^{th} bit of search-word.

$bl(n-1)$ = n^{th} bit of stored-word.

$$[sl(n) \odot bl(n)] = \{[sl(n) * bl(n)] + [\overline{sl(n)} * \overline{bl(n)}]\}$$

and

$$\overline{[sl(n) \odot bl(n)]} = \{\overline{[sl(n) * bl(n)] + [\overline{sl(n)} * \overline{bl(n)}]}\}$$

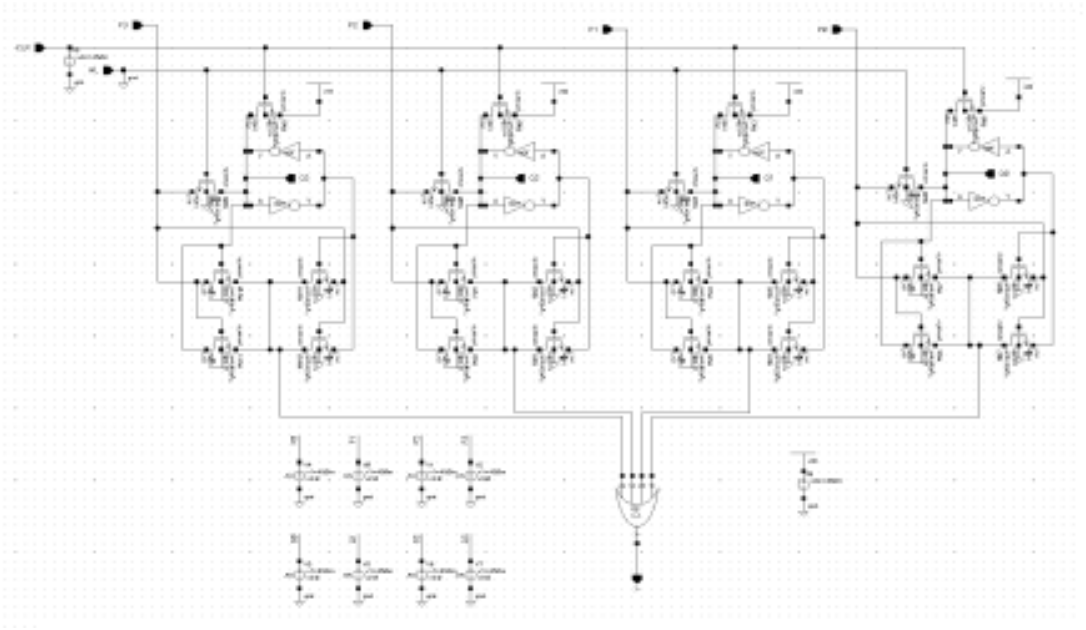

Figure 10. Static Parameter Comparison circuit using 45nm CMOS technology.

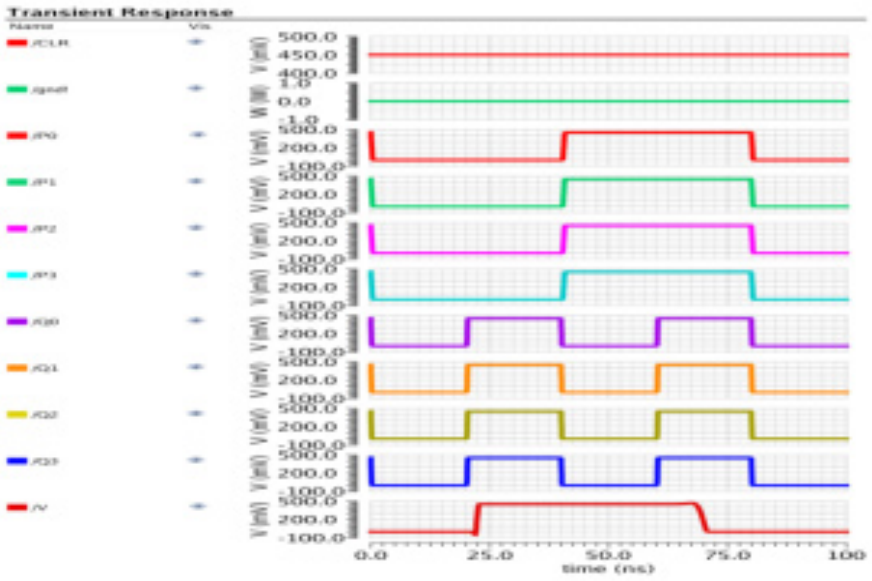

Figure 11. Transient response of Static Parameter Comparison circuit using 45nm CMOS technology.

In Figure.11 sl is A and bl is B .

The power consumption of the proposed Parameter Comparison circuit at 10-30MHz frequency in 45nm CMOS technology, at supply voltage of 0.45V is 0.02135µW for a 4x4 (4-bits from stored parameter-extracted data and 4-bits from input parameter-extracted data) size parameter comparison data at 10MHz.

6. Concept of MLSARL

In CAM, PB-CAM and TCAM different kinds of sense amplifiers are used. These sense amplifiers are used at every output of the memory row or column based on the circuit, to improve the strength of the stored and/or passing data in the CAM memory. Sense amplifiers consume

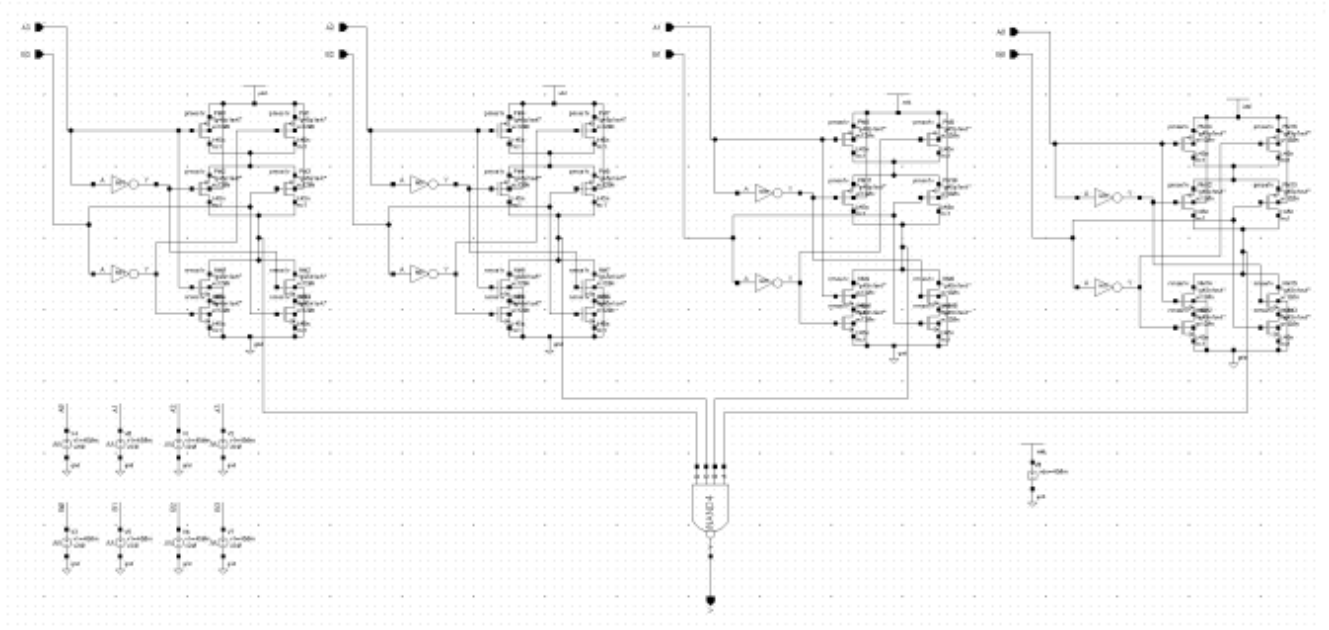

Figure 12. Proposed Parameter Comparison circuit using XNOR-NAND logic in 45nm CMOS technology.

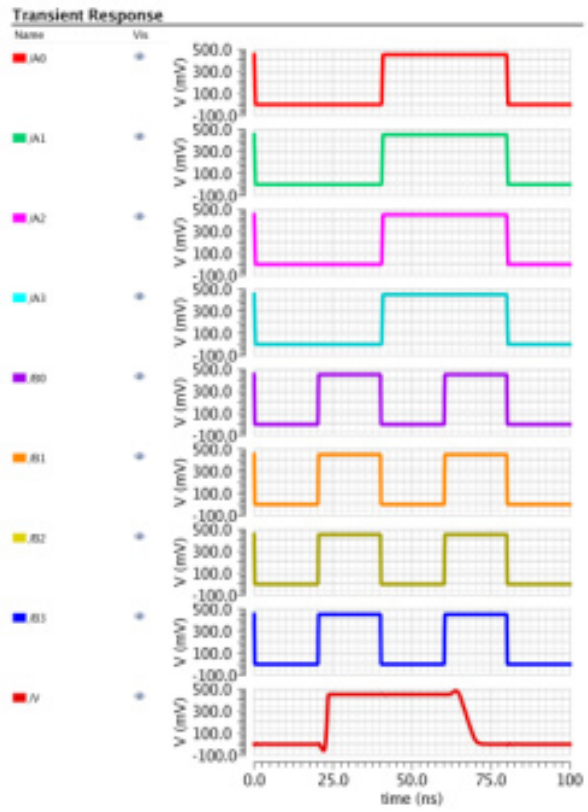

Figure 13. Transient response of proposed Parameter Comparison circuit using XNOR-NAND logic in 45nm CMOS technology.

more power during amplification process and leakage power is more. Therefore, by considering low-power, low-voltage, high-speed and more accurate amplification in PB-CAM, adopted Match Line Sense Amplifier with Resistive Load (MLSARL) scheme[7]. [Figure 14] shows the match line sense amplifier with resistive load using CMOS technology and [Figure 15] shows its transient analysis. For $l * k$ (l words, k bits) size of PB-CAM we need l number of MLSAs. These MLSA outputs are given to priority encoder. Priority encoder is connected between the MLSA output and Data-Match (PB-CAM output). During parameter comparison process, if more than one match is found then the priority encoder will take first match from those matches based on priority and sends or passes it to Data-Match line[12-16].

7. Concept of PB-CAM With MLSARL and Proposed Parameter Comparison Unit

PB-CAM is the most commonly used CAM in recent days. PB-CAM technique achieved by different kinds of Parameter Extractor (PE) and Parameter Comparison (PC) techniques. PE is developed by different techniques, such as ones-count, block-XOR, parity-bit and remainder functions. After extracting the parameter by using any

one of the PE techniques, the process of comparing the stored parameter and input parameter, before comparing the input data and stored data in the CAM is called *pre-computation* logic and it is called as PB-CAM. PB-CAM is mainly designed by ones count PE and static parameter comparison circuit[1]. In this paper implemented a PB-CAM with newly designed XNOR-NAND parameter comparison circuit. This newly implemented PB-CAM contains ones count parameter extractor, 7T PB-CAM cell, Match Line Sense Amplifier (MLSA) with resistive load and proposed XNOR-NAND parameter comparison circuit. [Figure 16] shows the PB-CAM with proposed parameter comparison circuit using CMOS technology. In Figure 16 the blocks represent, PE (parameter-extractor), PC (parameter-comparison circuit) and MLSA (match line sense amplifier with resistive load). The output waveforms of ones-count PB-CAM using MLSARL and proposed parameter comparison circuit is shown in [Figure 17].

8. Comparison of Power and Delay for Components of PB-CAM

This section mainly includes the comparative analysis of static parameter comparison circuit and proposed parameter comparison circuit with power and delay as main parameters, by using 180nm, 90nm and 45nm technologies in Cadence Virtuoso for different operations and calculated power consumption and delay values are shown in Table 4, Table 5, Table 6 and Table 7.

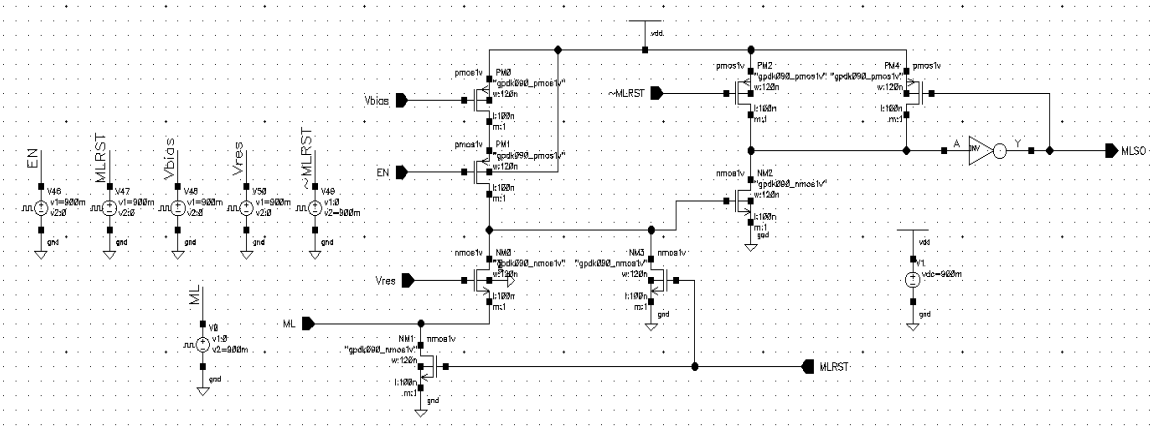

Figure 14. Match Line Sense Amplifier with Resistive load (MLSARL).

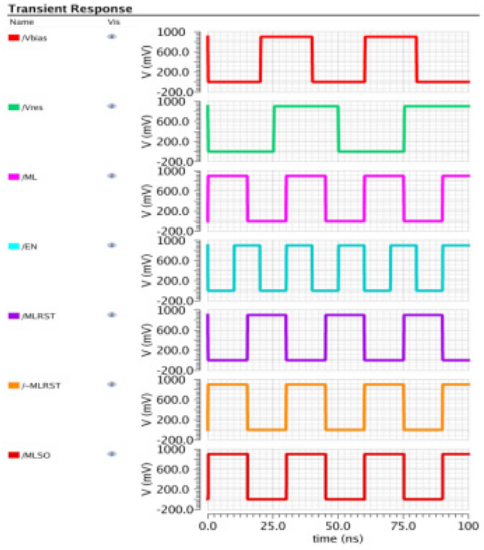

Figure 15. Transient response of MLSARL in 90nm CMOS technology.

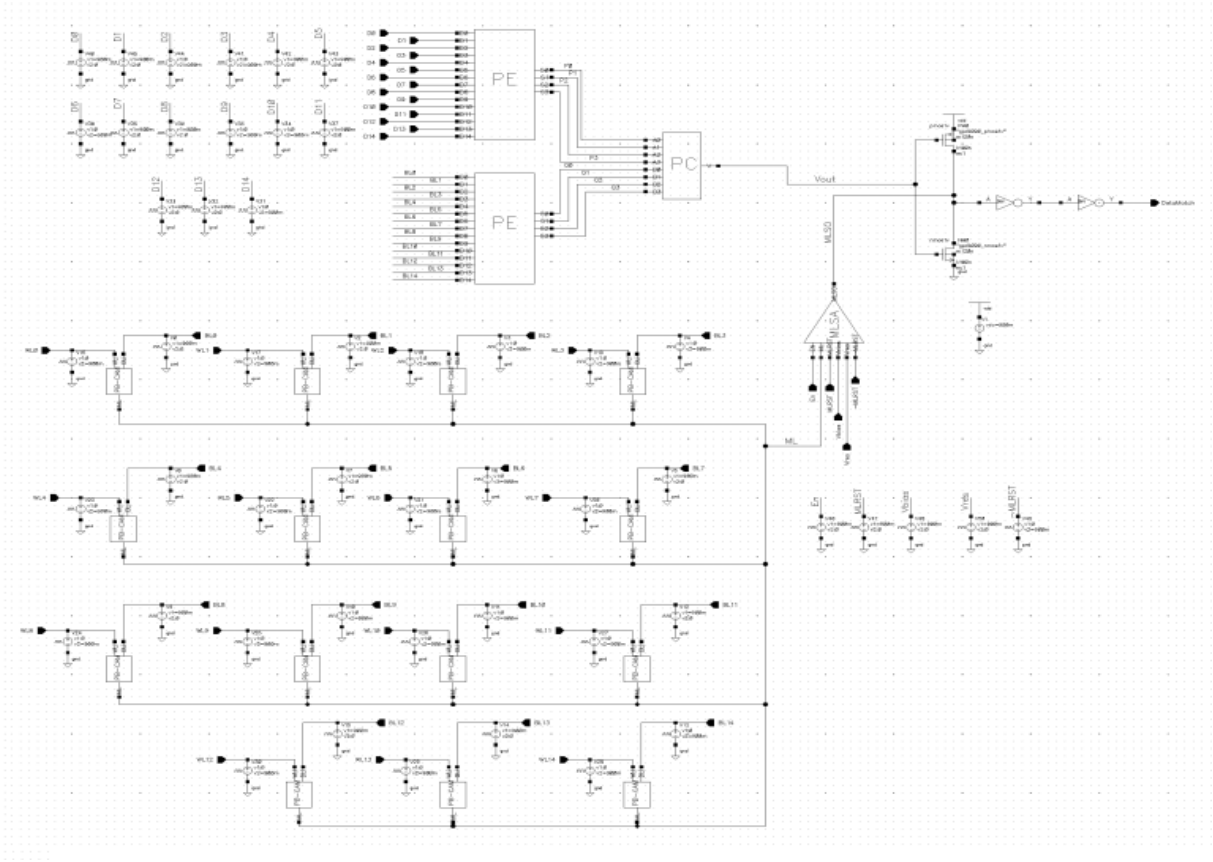

Figure 16. Ones-count PB-CAM with MLSARL and Proposed Parameter Comparison circuit.

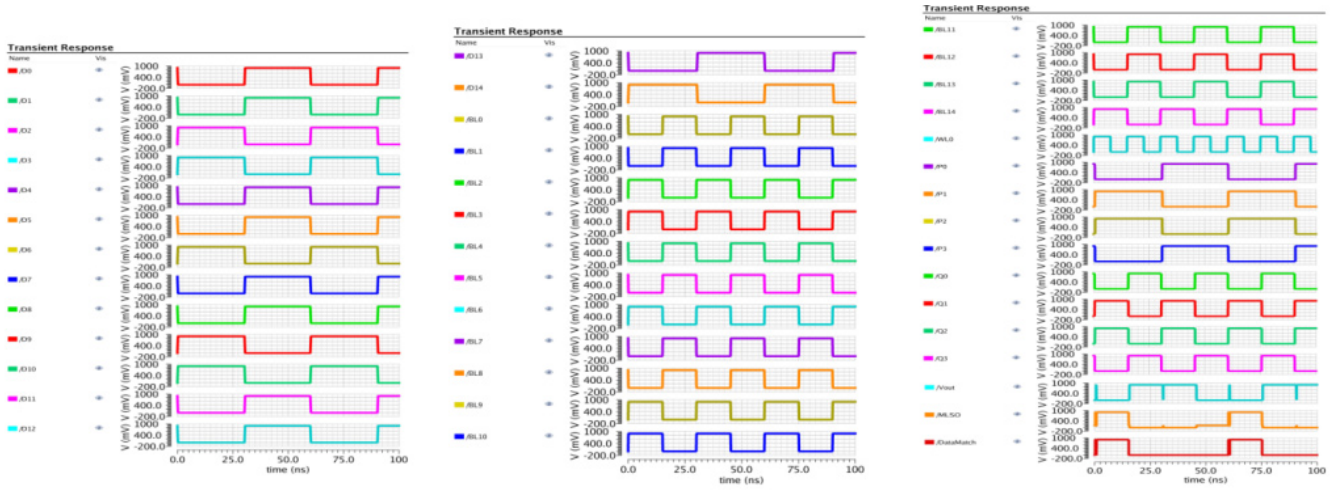

Figure 17. Transient response of Ones-count PB-CAM with MLSARL and proposed parameter comparison circuit in 90nm CMOS technology.

Table 4. Comparison for Delay and Power consumption of the Parameter Extractor using 180nm, 90nm and 45nm CMOS technology

Technology used (in nm)	Parameter Extractor by using Ones-Count Method (Delay in ns)	Parameter Extractor by using Ones-Count Method (Power in μW)
180	14.4	558
90	10.46	5.324
45	8.13	2.240

Table 5. Comparison for Power consumption of the static parameter comparison and proposed parameter comparison circuit using 180nm, 90nm and 45nm CMOS technology

Technology used (in nm)	Static Parameter Comparison circuit (Power in μW)	Proposed Parameter Comparison circuit (Power in μW)
180	31.87	21.32
90	5.805	0.582
45	0.03234	0.02135

Table 6. Comparison for Delay of the static parameter comparison and proposed parameter comparison circuit using 180nm, 90nm and 45nm CMOS technology

Technology used (in nm)	Static Parameter Comparison circuit (Delay in ns)	Proposed Parameter Comparison circuit (Delay in ns)
180	20.29	20.17
90	20.18	20.14
45	16.15	16.07

Table 7. Comparison for power and delay of the Ones-count PB-CAM with proposed parameter comparison circuit using 180nm and 90nm CMOS technology

Technology used (in nm)	Ones-count PB-CAM with Proposed Parameter Comparison circuit (Power in mW)	Ones-count PB-CAM with Proposed Parameter Comparison circuit (Delay in ns)
180	2261	30
90	0.1291	25.66

9. Conclusion

In this paper, a XNOR-NAND parameter comparison circuit for low power and high speed PB CAM was proposed. There has been many techniques evolved for designing CAM, PB-CAM and Parameter Extractor by holding the aim to achieve low power consumption, low-noise, high-speed, less hardware cost, less data comparisons and with minimum hardware requirements. We have discussed about Traditional Dynamic CAM architecture, Ones-Count PB-CAM, MLSARL, parameter extractor, static parameter comparison circuit, 9T CAM cell, and 7T PB-CAM cell and derived mathematical analysis for proposed parameter comparison circuit in PB-CAM. The proposed parameter comparison circuit was designed using Cadence 0.18μm, 0.09μm and 0.045μm with CMOS logic. For 128 words with 30bits each, PB-CAM with proposed parameter comparison circuit works up to 100MHz with less than 30mW power consumption at 1V supply and works up to 30MHz at 0.9V supply. The proposed Parameter comparison circuit consumes an average power of 0.02135μW in CMOS 45nm technology at supply of 0.45V.

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