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Switching Flow Graph Modelling of RRPP Based DC-DC Converter

Divya Navamani*, K. Vijayakumar A. Lavanya

EEE Department, SRM University; India, divyateddy1@gmail.com

Abstract

Objective: Small-signal modelling is a widespread analysis practice in power electronic converters which is used to fairly accurate the performance of non-linear devices with linear equations. The order of the dc-dc depends on the non-linear elements of the system. As the number of non-linear element of the converter is high, it's modelling and control becomes extremely complicated. Thus, there is a need for generalization of such converters by small signal modelling. Traditional modelling schemes using the averaging and small-signal linearization procedures are utilised for the advance modelling of the converters. **Method:** In this work, the purpose of the switching flow graph (SFG) and the Mason's gain formula aid the solution of the equations. The duty cycle to output and the input to output transfer functions are obtained. Those transfer function can be used for closed loop examination. **Findings:** Open loop analysis of the converter is done and the outcomes are verified through simulation. Theoretical and simulation results are shown to prove the accuracy of the developed small signal models. The derived topology is unstable in open loop condition. A prototype is developed to validate the performance of the proposed topology. **Improvement:** Closed loop analysis can be carried out with any type of controller.

Keywords: Loops, Modelling, Stability, Transfer Function, Voltage Gain

1. Introduction

The dynamic behaviour of the dc-dc converter can be easily studied by modelling methods. Modelling techniques are introduced in dc converters to design the closed loop system and to read the stability issues of the system. In the last three decades, many modelling is presented and implemented. Most predominantly used modelling techniques are the state-space averaging method, Current injected equivalent circuit approach[1,2] Unified Topological modelling[3], PWM switch modelling[4], the Alternate form of PWM switch model[5, 6] and so on. In 2010, L.K. Wong used Mason's gain formula to model the Sepic converter[7]. The method is found to be simple to derive the transfer function of the converter.

There are several transfer functions to learn the dynamic model of the converter. This paper obtains the key transfer function such as input to output transfer function and duty cycle to output transfer function of the derived topology. These two transfer functions are used to design the compensation model of the converter. There are 5 state variables in the derived topology. In the case of State Space Averaging Approach (SSA), inversion of the 5X5 matrix is a tedious and time consuming. So, the signal flow graph modelling technique is a simple for high order system[8]. Isolated[9, 15] and non-isolated DC-DC converters are used in many applications such as renewable energy system[10–13], Electric and Hybrid Vehicle[14] and so on.

This paper is constructed as follows: Section 2 initiates the proposed topology and its steady state analysis. Signal flow graph modelling and transfer function derivation is stated in section 3. Section 4 manifests the simulation and hardware results. Finally, the paper is summarized in section 5.

1.1 Steady state analysis of the proposed topology

The topology is derived by Reduced Redundant Power Processing (RRPP) technique. A family of configuration is

*Author for correspondence

offered for PFC regulator in[8]. In those 16 configurations, II-A configuration is chosen to derive a new topology with luo converter[9] and boost converter. Figure 1 gives the illustration of the suggested topology.

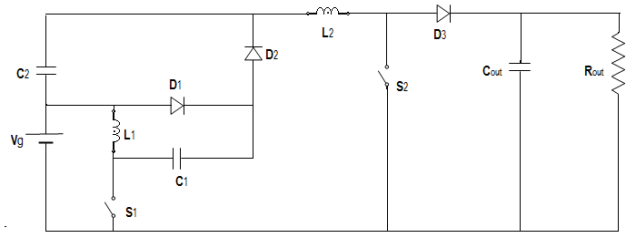


Figure 1. Proposed topology

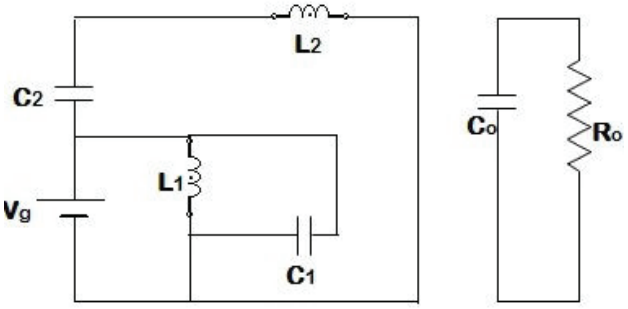
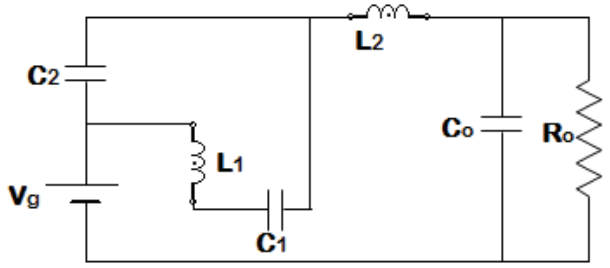


Figure 2. (a) Circuit under ON condition



(b) Circuit under OFF condition

Steady state analysis is carried out by volt-sec balance principle. Figure 2. (a) and (b) presents the circuit under on and off states respectively.

The state equations of ON state can be derived as follows

$$L_1\frac{d}{dt}\frac{d}{dt}i_{L1}=v\ v_{g}=v\ v_{C1} \quad (1)$$

$$L_2\frac{d}{dt}\frac{d}{dt}i_{L2}=v\ v_{g}+v\ v_{C2} \quad (2)$$

$$C_1\frac{d}{dt}v\ \frac{d}{dt}v_{C1}=i_g-i_{L1}-i_{L2} \quad (3)$$

$$C_2\frac{d}{dt}v\ \frac{d}{dt}v_{C2}=i_{L2} \quad (4)$$

$$C_0\frac{d}{dt}v\ \frac{d}{dt}v_{C0}=-i_0 \quad (5)$$

The state equations of OFF state can be derived as follows

$$L_1\frac{d}{dt}\frac{d}{dt}i_{L1}=v\ v_{C1}-v\ v_{C2} \quad (6)$$

$$L_2\frac{d}{dt}\frac{d}{dt}i_{L2}=v\ v_{g}+v\ v_{C2}-v\ v_{C0} \quad (7)$$

$$-C_1\frac{d}{dt}v\ \frac{d}{dt}v_{C1}=-i_g+i_{L1}+i_{L2} \quad (8)$$

$$C_2\frac{d}{dt}v\ \frac{d}{dt}v_{C2}=i_{L2}-i_{L1} \quad (9)$$

$$C_0\frac{d}{dt}v\ \frac{d}{dt}v_{C0}=i_{L2}-i_0 \quad (10)$$

1.2. Signal flow graph modelling

1.2.1 Perturbation and Small Signal linearization technique

The two inductors in the topology are averaged in on and off condition.

Inductor L_1 is averaged in on and off condition, and the DC and AC equations are separated.

$$sL_1(\tilde{i}_{L1}+I_{L1})=\tilde{V}_{c1}+V_{c1}-(1-D-d')\ d'\ (\tilde{V}_{C2}+V_{C2}) \quad (11)$$

DC equation: $\bar{V}\bar{V}_{C1}=(1-\bar{D}\ \bar{D})(\bar{V}\ \bar{V}_{C2})$

AC equation: $sL_1\tilde{i}_{L1}=\tilde{V}_{c1}-(1-\bar{D}\ \bar{D})\tilde{V}_{C2}+\tilde{d}\tilde{d}(V_{C2})$

Inductor L_1 is averaged in on and off condition, and the DC and AC equations are separated.

$$sL_2(\tilde{i}_{L2}+I_{L2})=\tilde{V}_g+V_g+\tilde{V}_{C2}+V_{C2}-(1-D-d')\ d'\ (\tilde{V}_0+V_0) \quad (12)$$

DC equation: $\bar{V}\bar{V}_g+\bar{V}\bar{V}_{C2}=(1-\bar{D}\ \bar{D})(\bar{V}\ \bar{V}_0)$

AC equation: $sL_2\tilde{i}_{L2}=\tilde{V}_g+\tilde{V}_{C2}-(1-\bar{D}\ \bar{D})\tilde{V}_0+\tilde{d}\tilde{d}(V_0)$

Capacitor C_1 is averaged in on and off condition, and the DC and AC equations are separated.

$$sC_1(\tilde{V}_{c1}+V_{c1})=\bar{\bar{i}}\bar{\bar{i}}_g+I_g-(\bar{\bar{i}}\bar{\bar{i}}_{L1}+I_{L1})-(\bar{\bar{i}}\bar{\bar{i}}_{L2}+I_{L2}) \quad (13)$$

DC equation: $\bar{I}\bar{I}_g=\bar{I}\bar{I}_{L1}+\bar{I}\bar{I}_{L2}$

AC equation: $sC_1\tilde{V}_{C1}=\bar{\bar{i}}\bar{\bar{i}}_g-\bar{\bar{i}}\bar{\bar{i}}_{L1}-\bar{\bar{i}}\bar{\bar{i}}_{L2}$

Capacitor C_2 is averaged in on and off condition, and the DC and AC equations are separated.

$$sC_2(\tilde{V}_{c2}+V_{c2})=(\bar{\bar{i}}\bar{\bar{i}}_{L2}+I_{L2})-(\bar{\bar{i}}\bar{\bar{i}}_{L1}+I_{L1})(1-D-d')\ d' \quad (14)$$

DC equation: $-\bar{I}\bar{I}_0+(1-\bar{D}\ \bar{D})\ \bar{I}\ \bar{I}_{L2}=0$

AC equation: $sC_0\tilde{V}_{C0}=-\bar{\bar{i}}\bar{\bar{i}}_0+(1-\bar{D}\ \bar{D})\ \bar{i}\ \bar{i}_{L2}-I_{L2}\tilde{d}\tilde{d}$

Capacitor C_O is averaged in on and off condition, and the DC and AC equations are separated.

$$sC_0(\tilde{V}_{c0}+V_{c0}) = -\tilde{I}\tilde{I}_0 - I_0 + (1-D-\tilde{d}')\,\tilde{d}'\,(\tilde{I}\tilde{I}_{L2}+I_{L2}) \quad (15)$$

DC equation: $\tilde{I}\tilde{I}_{L2} - \tilde{I}\tilde{I}_{L1}(1-\tilde{D}\,\tilde{D}) = 0$

AC equation: $sC_2\tilde{V}_{C2} = \tilde{I}\tilde{I}_{L2} - (1-\tilde{D}\,\tilde{D})\,\tilde{I}\tilde{I}_{L1} + I_{L1}\tilde{d}\,\tilde{d}$

By taking the Laplace transform of the differential equations governing the system, AC equations can be derived. The constants and variables of s domain equations are identified as input, output, and intermediate variables. For every variable, a junction is designated in the graph. For each equation, a signal flow graph is sketched, and they are interconnected to provide overall signal flow diagram of the system. The AC equations written above are employed to develop a switching flow graph as shown in figure 3. All the independent states are characterized by the nodes, and the gain of the every path between the nodes can be received from the AC equations.

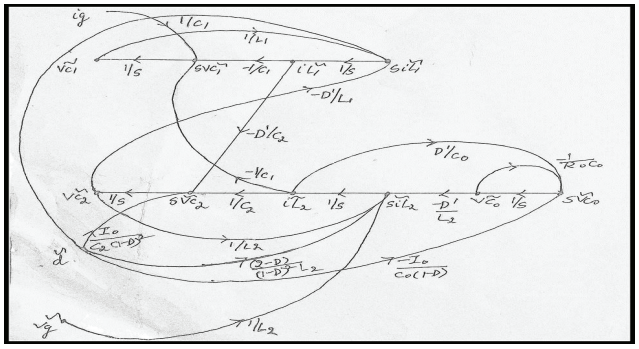


Figure 3. Signal flow graph of proposed topology

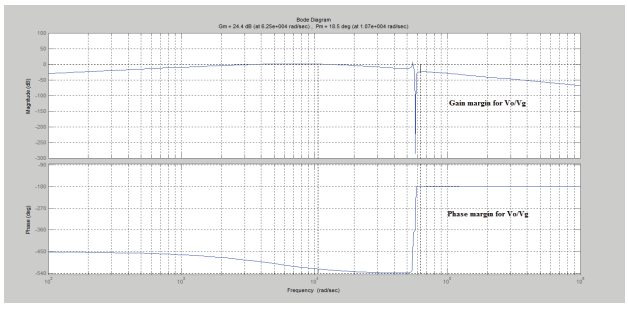


Table 1. Loops in signal flow graph

Table 1. Loops in signal flow graph

Individual loops	Two non-touching loops	Three Non Touching Loops
Loop 1:$\tilde{v}c_0 \rightarrow s\tilde{V}_{C0} \rightarrow \tilde{V}_{C0}$ $L_1 = (-1/sR_0C_0)$	L_1 & L_3 : $(-1/s^3R_0C_0L_2C_2)$	L_1, L_4, L_3 : $(1/s^5R_0C_0L_1L_2C_1C_2)$
Loop 2:$\tilde{i}_{L2} \rightarrow s\tilde{V}_{c0} \rightarrow \tilde{V}_{C0} \rightarrow s\tilde{i}_{L2} \rightarrow \tilde{i}_{L2}$ $L_2 = (-D'^2/s^2L_2C_0)$	L_1& L_4 : $(1/s^3R_0C_0L_1C_1)$	
Loop 3:$\tilde{V}_{C2} \rightarrow s\tilde{i}_{L2} \rightarrow \tilde{i}_{L2} \rightarrow s\tilde{V}_{C2} \rightarrow \tilde{V}_{c2}$ $L_3 = (1/s^2L_2C_2)$	L_1 & L_5 : $(-D'^2/s^3R_OC_0L_1C_2)$	
Loop 4:$\tilde{V}_{c1} \rightarrow s\tilde{i}_{L1} \rightarrow \tilde{i}_{L1} \rightarrow s\tilde{V}_{c1} \rightarrow \tilde{V}_{c1}$ $L_4 = (-1/s^2L_1C_1)$	L_1 & L_6 : $(-D'/s^5R_0C_0L_1L_2C_1C_2)$	
Loop 5:$s\tilde{V}_{C2} \rightarrow \tilde{V}_{C2} \rightarrow s\tilde{i}_{L1} \rightarrow \tilde{i}_{L1} \rightarrow s\tilde{V}_{C2}$ $L_5 = (D'^2/s^2L_1C_2)$	L_2 & L_5 : $(-D'^4/s^4L_1L_2C_2C_0)$	
Loop 6:$\tilde{i}_{L2} \rightarrow s\tilde{V}_{C1} \rightarrow \tilde{V}_{C1} \rightarrow s\tilde{i}_{L1} \rightarrow \tilde{i}_{L1} \rightarrow s\tilde{V}_{C2} \rightarrow \tilde{V}_{C2} \rightarrow s\tilde{i}_{L2} \rightarrow \tilde{i}_{L2}$ $L_6 = (D'/s^4L_1C_1L_2C_2$	L_2 & L_4 : $(D'^2/s^4L_1C_1L_2C_0)$	
	L_3 & L_4 : $(-1/s^4L_1L_2C_1C_2)$	
Denominator Δ is, $\Delta = ((s^5R_0C_0L_1L_2C_1C_2) - [(-s^4L_1L_2C_1C_2) + (-s^3D'^2L_1C_1C_2R_0) + (s^3L_1C_1R_0C_0) + (-s^3L_2C_2R_0C_0) + (s^3D'^2L_2C_1R_0C_0) + (sD'R_0C_0)] + \{(-s^2L_1C_1) + (S^2L_2C_2) + (-s^2D'^2L_2C_1) - 1 + D + (-sC_1R_0D'^4) + (sD'^2R_0C_2) + (-sR_0C_0)\} - (1))$ / $(s^5R_0C_0L_1L_2C_1C_2)$		

By analysing the graph in figure 3, there are 6 individual loops and 7 two non-touching loops and 1 three non-touching loops. Using Mason's gain formula, the denominator and numerator of the transfer function is obtained as shown in Table 1 and Table 2 respectively.

Table 2. Numerator of the transfer function

Parameter	Vo/Vg	Vo/d
No of forward path	k = 1	k = 4
Path gain	$P_1 = D'/s^2L_2C_0$	$P_1 = -I_O/sC_O(1-D)$ $P_2 = (2-D)\,D'/s^2C_O(1-D)$ $P_3 = I_OD'/s^3C_OL_2C_2(1-D)^2$ $P_4 = -VgD'2/s^4C_OL_1L_2C_2D'$
Loops not touching the for forward path	$Ä_1 = 1 - [(D'^2/s^2L_1C_2) + (-1/s^2L_1C_1)]$	$\Delta_1 = 1 - ((1/s^2L_2C_2) - (1/s^2L_1C_1) + (D^{2'}/s^2L_1C_2) + D'/s^4L_1L_2C_1C_2)) + ((1/s^2L_2C_2) - (1/s^2L_1C_1))$
		$\Delta_2 = 1 - ((-1/s^2L_1C_1) + (D^{2'}/s^2L_1C_2))$ $\Delta_3 = 1 - (-1/s^2L_1C_1)$ $\Delta_4 = 1$

1.2.2. Designing of the converter:

The converter is designed with the following circuit parameters for simulation and hardware: Vg = 10 V, R=130 Ω; D = 0.3, Switching frequency (fs) = 60 kHz, Capacitors Co, C_1 and C_2 =10μF. Inductors are calculated with the derived equation (16) and (17).

$$L_1 = \frac{(1-D)^4 D R_L}{2(2-D)f_s} \quad (16)$$

$$L_2 = \frac{(1-D)^2 D R_L}{2f_s} \quad (17)$$

The Values of the inductors are L_1=22 μH, L_2=135 μH. By substituting the values input to output and control to output transfer functions are derived.

$$TF_1 = \frac{\widetilde{V_0}}{\widetilde{V_g}} = \frac{0.369X10^9S^3 + 1.225X10^{18}S}{S^5 + 769.2S^4 + 2.7X10^9S^3 + 2X10^{12}S^2 - 0.81X10^{18}S - 3.7X10^{21}} \quad (18)$$

$$S^5 + 769.2S^4 + 2.7X10^9S^3 + 2X10^{12}S^2 - 0.81X10^{18}S - 3.7X10^2$$

Equation (18) and (19) gives the transfer function required for designing the compensation circuit.

1.3. Simulation and Hardware results

Stability analysis of the proposed topology is studied by obtaining bode plot and pole-zero map in MATLAB/ Simulink. Figure 4 (a)-(d) gives the Bode plot and pole-zero map of the transfer function. Matlab coding is recorded in m file, and it is simulated, and the results are offered in figure 4.

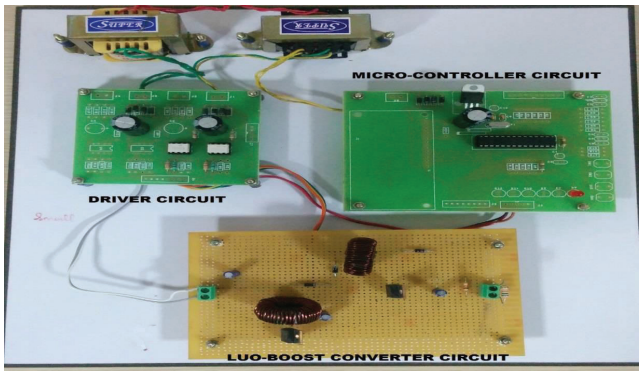
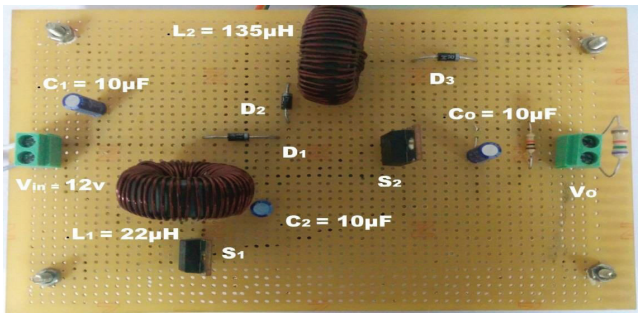
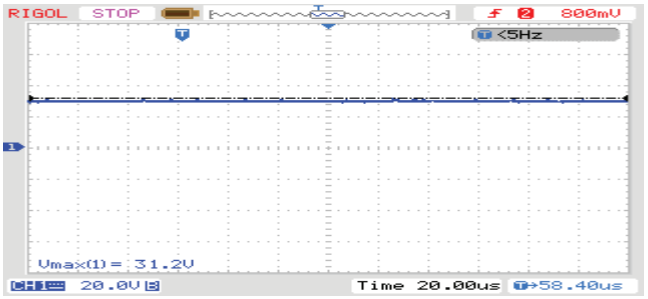


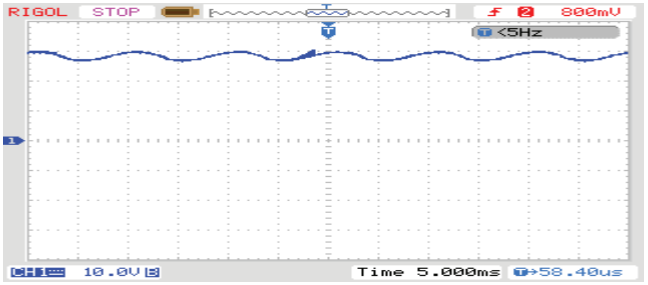
Figure 4. (a) Bode Plot for the transfer function Vo/Vg



(b) Poles and Zeros plot for the transfer function Vo/Vg



(c) Bode Plot for the transfer function Vo/d



(d) Poles and Zeros plot for the transfer function Vo/d

The steadiness of the converter can be measured by determining the poles and zeroes of the derived transfer function and sketching the Bode plot of the transfer function. From the Bode plot, gain and phase margin are noted. The gain margin input to output voltage transfer function is 24.4 dB and phase margin is 18.5 degree. The gain margin and phase margin of control to output voltage transfer function are -53.2 dB and -85.5 degree respectively. If the phase margin is low and negative, the system is unstable. There is one zero in the right half of the S- plane in both the transfer function. These two conditions conclude that the system is unstable. The compensating circuit can be derived with the help of these transfer function.

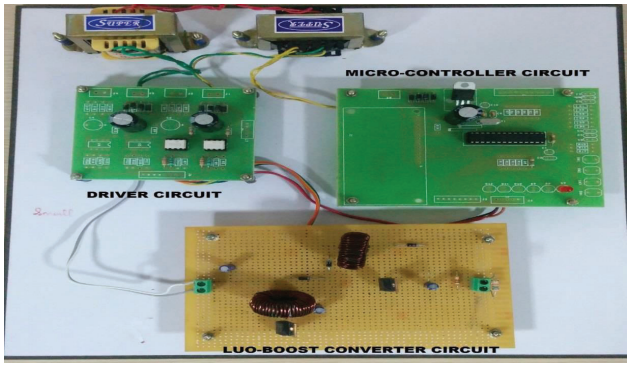
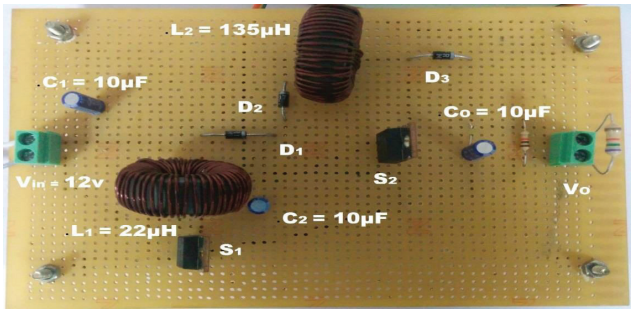
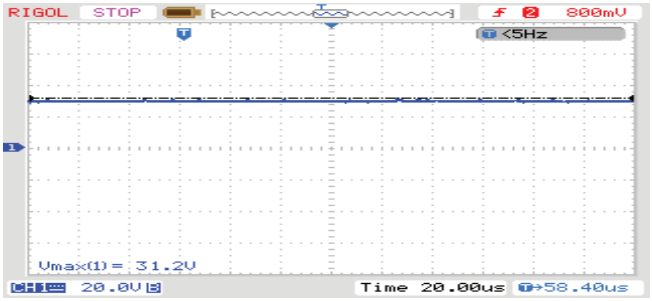


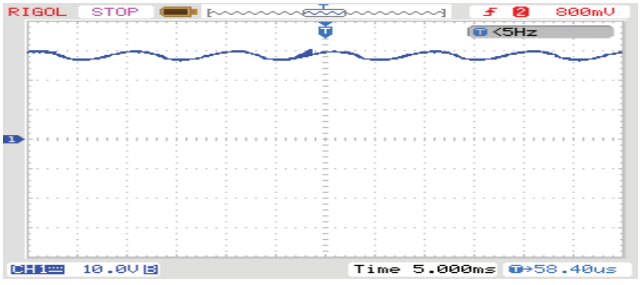
Figure 5. (a) Photograph of complete circuit



(b) Photograph of Proposed topology



(c) Output voltage



(d) Output capacitor voltage

A prototype is developed to validate the effectiveness of the converter. The output voltage is measured for D=0.3, and it is found to 31 V as shown in figure 5(c). Due to the parasitic components, hardware results are less than the calculated results. Conventional boost converter with the same circuit parameters provides an output of 14 V. With the derived topology, voltage gain of the converter is increased. Figure 5(a) and (b) gives the photograph of the derived converter. Figure 5(d) shows the voltage across the output capacitor.

2. Conclusion

The proposed converter gives a high voltage boost even for low power input. Research indicates that these can even be used in applications where the variable load is needed. Transfer functions of the proposed DC-DC converters are obtained by the mason's gain formula and it is presented in this work. Averaging and small signal linearization techniques have been applied, and the measures of deriving transfer functions from the core state equations have been presented. The utilize of the signal flow graph and the Mason's gain formula helps to solve composite high order symbolic equations step by step. This allows us to handle many state variables in a convenient way. The duty cycle to output and the input to output transfer functions have been derived. The converter circuit is designed, simulated in MATLAB and the bode-plot has been found out to read the stability of the system. The boosting of the voltage of the derived topology has been implemented and validated using hardware.

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