

VLSI based Design of an Efficient Hybrid Watermarking Scheme for Multimedia Content Protection

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Abstract

Background/Objectives: In this paper, a new concept of hybrid DWT-SVD watermarking scheme for the secure transit of multimedia information like text, image, audio and video is presented. Resolving the copyright protection problem of colour videos and to provide effective authentication. **Methods/Statistical Analysis:** My proposed work algorithms can be tested in VLSI (Very Large Scale Implementation) boards that can supported for the design generated by this hybridization methodology also been reviewed. **Findings:** This concept will produce the best results in terms of performance metrics like MSE, PSNR etc. than other domains and transformations and as future enhancement it can use Cadence/Xilinx ISE System Generator (SysGen) to generate IC and then implemented in Altera Quartus II FPGA. **Improvement/Application:** We developed a new source code for video watermarking using hybrid DWT-SVD which will be useful in variety of applications. It's being effective and proven by comparing it with existing image watermarking using hybrid DWT-SVD has been examined and the Proposed design is simulated using MATLAB (Matrix Laboratory).

Keywords: Cover Video, Hybrid DWT-SVD, Image, MATLAB, Watermark

1. Introduction

In this paper, a hybrid video watermarking algorithm using DWT (Discrete Wavelet Transformation)-SVD (Singular Value Decomposition) is proposed for the multimedia content like text, image, audio and video protection. The DWT-SVD based hybridization methodology, which are developed to improve the real time authentication². In addition, the FPGA (Field Programmable Gate Array) implementation of the proposed design can be done in future which will achieve the proposed watermarking concept. Compared with the previous watermarking techniques the rigidity of the proposed scheme will provide

low power, robust and secure transmission of multimedia content among the internet such as the low cost of system hardware, the increase in computing power and storage capacity and the massive growth in data size generated by digital media (images, video, audio). To this end, still the main challenge in the hybrid video watermarking is how to effectively embed, extract, analyze and implement in VLSI. The effective applications where the proposed algorithm used are Ownership demonstration/ Copyright protections on Multimedia, Defence application, Authentication or Tamper detection, Broadcast monitoring, Content labelling, Copy control or Access control, Annotation, Content protection³.

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2. Aim and Scope of Present Investigation

Video watermarking using hybrid transformation is a software framework for solving many multimedia content problems. By using the Verilog HDL/VHDL programming model, it can be processed in FPGA12. DWT-SVD Hybridization has the two main functions Embedding and Extraction.

This procedure will make a review on previous watermarking concepts. It will be classified on the following basis:

- Watermark insertion domain: Spatial, Transform or Frequency Domain Techniques.
- Type of document: Text, Image, Audio, Video.
- Watermark detection and extraction: Blind, Non-blind Watermarking.
- Ability of watermark to resist attack: Fragile, Semi-fragile Watermarking.
- Visibility/Human Perception: Visible, No visible or Invisible Watermarks.
- Invisible watermarks: Robust, Fragile. Robust: Private, Public and Invertible, Non-invertible, Quasi-invertible, Non quasi-invertible.
- Application: Source based, Destination based.

The goal for this watermarking concept is to perform transmission without any loss of data and to provide high level security. This should be done in matlab environment. The source code generated should meet the designer constraints.

3. Proposed Methodology

3.1 Existing System

In the past the watermarking using LSB (Least Significant Bit), DCT (Discrete Cosine Transform) etc. is performed. These previous works will have several drawbacks and less robustness. So, combining DWT (Discrete Wavelet Transformation) and SVD (Singular Value Decomposition) transforms¹ has been introduced and done for image to image watermarking. This concept will produce the best results than other domains and transformations.

3.2 Proposed System

In proposed system as a continuation of existing work,

image into video watermarking scheme using hybrid DWT-SVD transformation is performed and analyzed.

4. Hybrid Video Watermarking Framework

4.1 Video Watermarking

The Embedding and Extraction framework is done as follows:

4.1.1 Embedding Process Flow

- Input color video is selected and the watermark image is chosen to hide with video.
- Video is splitted into number of frames for fast execution and high accuracy.
- Frame to image conversion is done and the DWT is applied on it.
- As a result of DWT, we will be obtaining the LL, LH, HL and HH bands respectively. LL band contains the information and robust than other bands.
- SVD is applied to each of the subband coefficients to get the singular values.

4.1.2 Extraction Process Flow

- By taking IDWT, we will be getting the extracted watermark video.
- We can extract cover video as result of inverse DWT-SVD hybrid transform.
- Resultant watermarked image will be produce in all the four wavelet subbands.
- The effectiveness of this methodology is verified by performance factors like PSNR (Peak Signal-to-Noise Ratio), MSE (Mean Squared Error) factors.
- Extraction process completed with low MSE and higher PSNR will be the proof for the highly robust video watermarking.

4.2 Advantages of Hybridization Scheme

It provides the better level of security compared to various transforms.

- Imperceptibility – high hiding capacity
- Unambiguous
- Less computational complexity
- Interoperability

- High robustness and protection against various attacks like noise addition, rotation, cropping, scaling, filtering, resizing and compression
- Overcome drawbacks of spatial domain watermarking concepts.


4.3 DWT-SVD Hybridity for Videos with Images

It is a local transformation from time and frequency domain and easily generates a variety of different resolution images³. It decomposes the given input video into four multi-resolution subbands, namely, LL, LH, HL and HH. A high-frequency subband contains the edge information of input video and LL subband contains the clear information about the video. Applied on luminance component of each frame and reconstruction is obtained by IDWT (Inverse Discrete Wavelet Transform). The high frequency sub band coefficients are selected for embedding watermark image within a cover image after SVD applied to that subbands¹³. SVD is an effective tool for data transfer. Singular values have good stability. Quality is retained even after addition of small values. The subbands are lower resolution approximation image (LL) as well as horizontal (HL), vertical (LH) and diagonal (HH) detail components.

4.4 Quality Measures

The Performance of the proposed algorithm is effectively rated based on the following video and image quality metrics. Key parameters like PSNR (Peak Signal to Noise Ratio-dB), MSE (Mean Squared Error) has been calculated.

5. Software Analysis

Matlab®  tool is used for performing software end simulation.

5.1 Hybrid Image with Image Watermarking Existing Work

The following is the framework for hiding image into image

- Select the input image Figure 1.
- Input image is been converted to gray scale in Blue plane Figure 2.

- DWT-SVD is performed on the B plane image Figure 3
- Logo or watermark image is selected Figure 4.
- Completion of embedding process Figure 5.
- Reconstruction is done by applying IDWT Figure 6.
- Extraction side – Retrieval of the hidden image Figure 7.
- Performance metrics like MSE, PSNR calculated for the entire transmit and receive process Figure 8.
- Values calculated for image watermarking using DWT-SVD:
 - dec = Watermarked;
 - [M N] = size (dec);
 - $MSE = \frac{\sum (\sum ((X - dec).^2))}{(M*N)}$;
 - $PSNR = 10 * \log_{10} (255*255/MSE)$;
 - M, N is the size of row and column pixels respectively.
 - LL: 485.5000, LH: 106.5000, HL: 104.0000, HH: 44.000

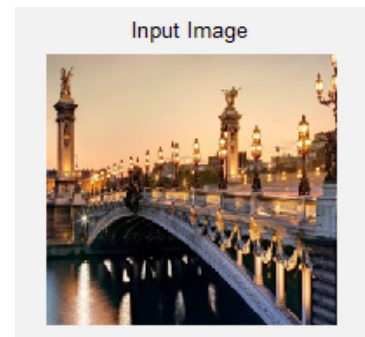


Figure 1.

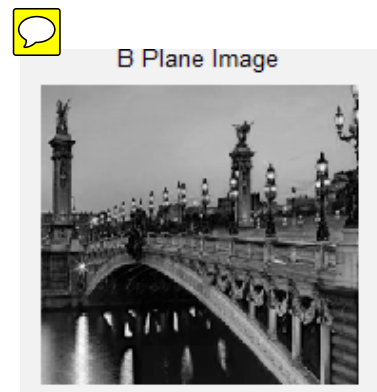


Figure 2.



Figure 3.

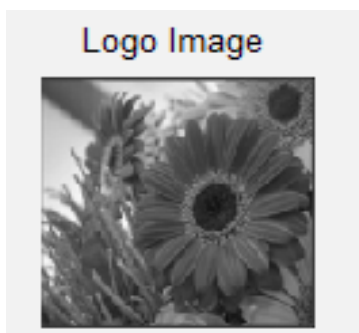


Figure 4.

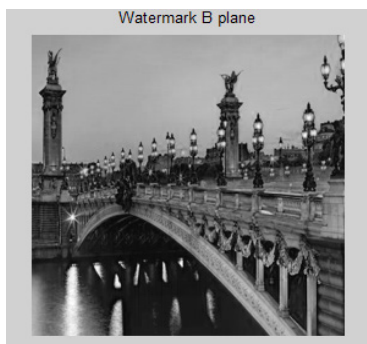


Figure 5.

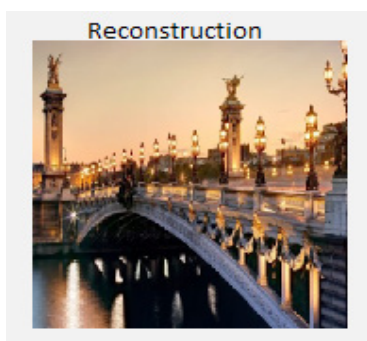


Figure 6.



Figure 7.

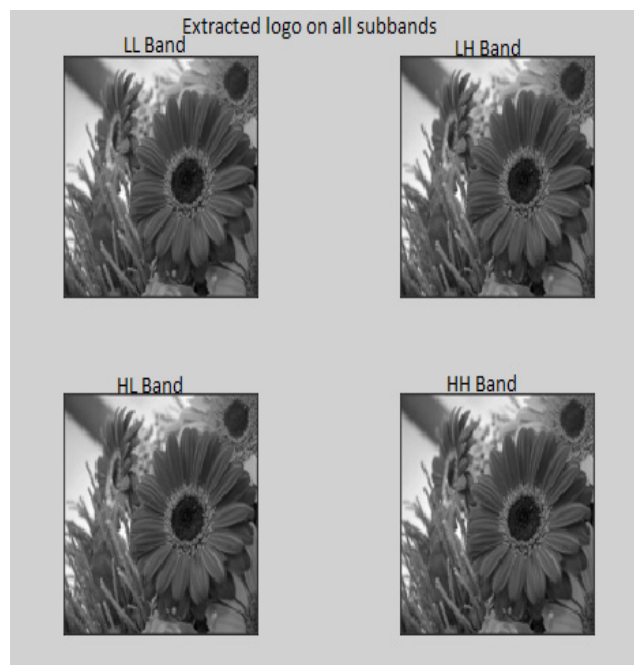


Figure 8.

Determination of Performance Validation Factors

MSE	0.42907
PSNR	51.8055

6. Simulation Results and Observations for Proposed Video Watermarking Using Hybrid DWT-SVD

6.1 Steps as Follows

- Input video file is chosen Figure 9.
- Video gets splitted into frames and stored as jpg format - No. of frames to be given for faster resolution Figure 10-13.
- Frames splitting process gets completed.
- Original video displayed with noise removal Figure 14.
- DWT performed; LLband used for further processing Figure 15.
- Watermark image to hide with video is selected Figure 16.
- Reconstruction of cover video by IDWT - Extracted watermark video Figure 17.
- Extracted watermark Figure 18.
- Values calculated for video watermarking using dwt-svd:
 - $Q = 255$;
 - $MSE = \frac{\sum (\sum ((\text{uint8}(\text{rgbout}) - \text{rgbimage}).^2))}{r/c}$;
 - $PSNR = 10 * \log_{10}(Q/MSE)$;
 - r, c is the size of row and column pixels respectively.
 - LL: 510.0000, LH: 199.5000, HL: 133, HH: 70.
- Sub band data's show the effectiveness of proposed video watermarking compared to other concepts.

Input video



Figure 9.

Frame 1



Figure 10.

Frame 2

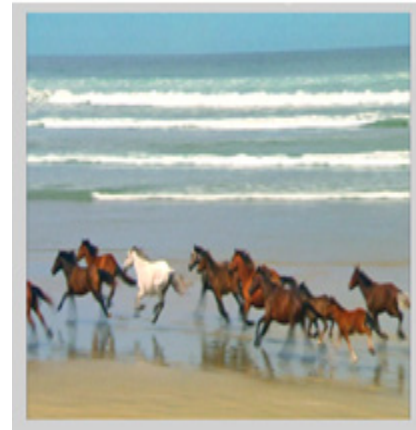


Figure 11.

Frame 3



Figure 12.

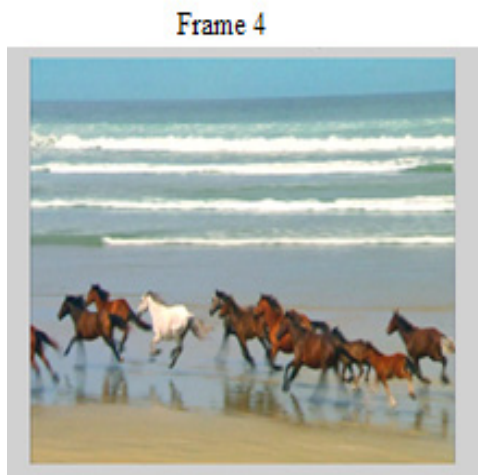


Figure 13.



Figure 16.

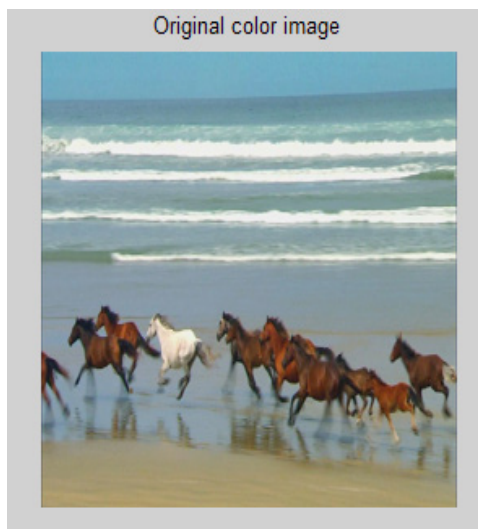


Figure 14.



Figure 17.

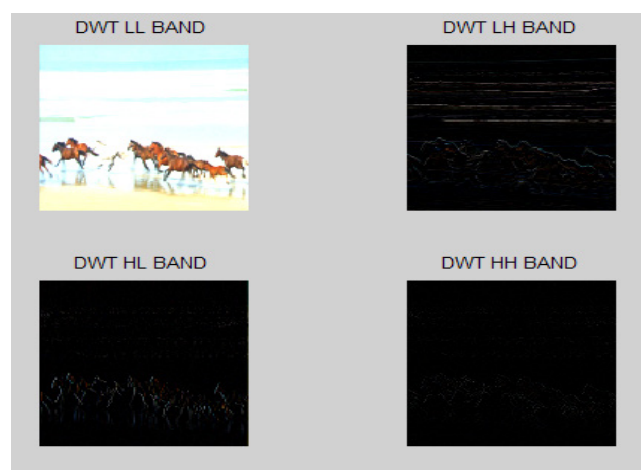


Figure 15.

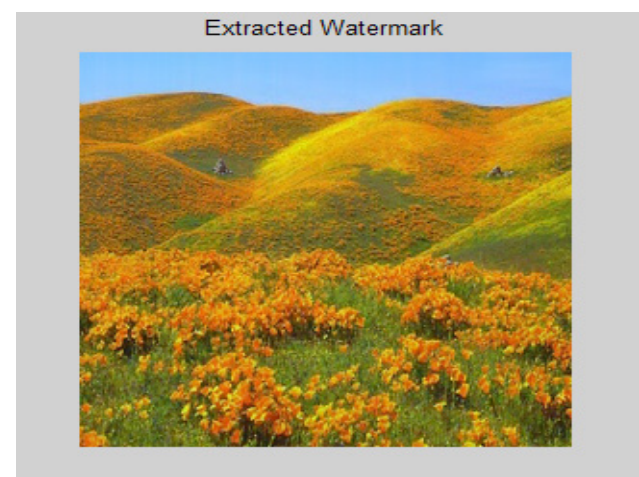


Figure 18.

Value added metrics for proposed code result:

The PSNR performance is 46.4783 dB

MSE performance is 0.0057.

7. Survey on Hardware Implementation

Matlab or Simulink models are converted to HDL (Hardware Description Language) for mapping it to Xilinx Altera boards⁷. With the proposed work, VLSI architecture implementation can be done and it should be designed in such a way to perform the system with low power, high speed, less area and good timing constraints in order to yield high-performance. Low-power VLSI features, such as multiple supply voltages, dynamic clocking, and clock gating will be considered. High performance architectural implementations, such as pipeline or parallelism, are under research. This hardware implementation can be tested by generating chip for each block used in proposed algorithm and interfacing it with the FPGA kit⁹. It can achieve accuracy, noise also the speed in computation and low power consumption also.

7.1 Board Design for the Proposed Algorithm

The Processors are completely code and pin compatible, differing only with respect to their performance and on-chip memory. By integrating a rich set of industry-leading system peripherals and memory, processors are the platform of choice for next generation applications that require RISC (Reduced Instruction Set Computers)-like programmability, multimedia support, and leading-edge signal processing in one integrated package. Processor is highly integrated system-on-chip solutions for the next generation of digital communication and customer multimedia application. By combining industry-standard interfaces with a high performance signal processing core, users can develop cost-effective solutions quickly without the need for costly external components. The system peripherals include a UART port, an SPI (Serial Peripheral Interface) port, two Serial Ports (SPORTS), four general-purpose timers (three with PWM (Pulse Width Modulation) capability), a real-time clock, a watchdog timer, and a parallel peripheral interface. Processor core, memory unit, real-time clock, DMA (Direct Memory Access) controllers, watchdog timer, UART (Universal Asynchronous Receiver Transmitter) port, booting modes, flash mem-

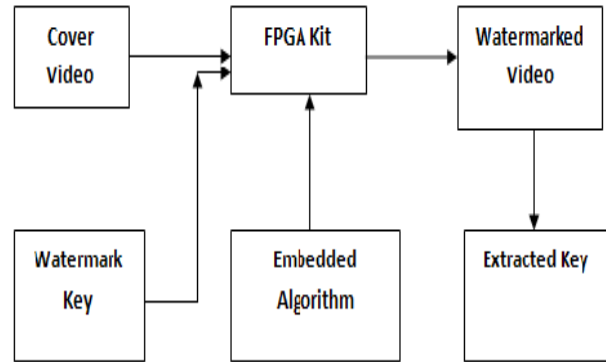


Figure 19. Block diagram.

ory, SDRAM (Synchronous Dynamic Random Access Memory) are the key parts to be presented in the board. Figure 19 is rough block diagram for future work.

8. Conclusion and Futurework

This paper introduces the new concept of video watermarking using hybrid transformation which can be applied in many fields including copyright issues and video conferencing.

As future enhancement, we can make the simulink blocks for this proposed design and mapping of HDL to field programmable gate array boards can be done. This will prove the effectiveness of the proposed algorithm at higher level hardware implementations.

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